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High Voltage DC Switchgear Development For Multi-KW Space Power Systems

FINAL REPORT
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16. Abstract

This report relates the design, development and evaluation of three types of Solid State Power Controllers (SSPC's) for High Voltage, High Power DC system applications. The first type was rated at 25A, 500-1100VDC and utilized a SCR power switch. The second type was rated at 80A, 200-400VDC and employed an electromechanical power switch element with solid state commutation. The third type was rated at 50A, 200-400VDC utilizing a transistor power switch.

Significant accomplishments included high operating efficiencies (some exceeding 99.5%), fault clearing, high/low temperature performance and vacuum operation. These and other test results are included in this report.

Included in Section I are recommendations for the future and the specifications for the three HVDC SSPC's are included in the Appendices.

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FOREWORD

The work described in this report was performed by the Electrical Systems Division of Westinghouse Electric Corporation in Lima, Ohio. The work was performed under contract number NAS3-21755 with the National Aeronautics and Space Administration (NASA). The project was managed by Messrs. John Sturman and Gale Sundberg of the Electric Propulsion and Space Experimental Branch, NASA-Lewis Research Center in Cleveland, Ohio.

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SECTION I

SUMMARY

1.1 Project Synopsis

This report summarizes the experience gained in developing and applying Solid State Power Controller (SSPC) technology at high voltage DC (HVDC) potentials and power levels of up to 25 KW. This program extended from January, 1979, through June, 1981, under the direction of the NASA-Lewis Research Center on contract NAS3-21755. The program consisted of seven tasks which are summarized as follows.

The PRELIMINARY ANALYSIS AND TRADE-OFF STUDIES, Tasks I and II, focused on HVDC switching devices and power switching concepts. Emphasis was placed on selecting devices and circuit concepts that would meet the performance requirements and stresses encountered in HVDC load switching applications.

The DESIGN ANALYSIS, FABRICATION AND EVALUATION, Tasks III through V, resulted in the design and development of three types of HVDC switchgear:

a. 25A/1 KVDC SCR-type power switch SSPC;

b. 80A/400 VDC "Hybrid" electro-mechanical solid state circuit breaker (EM/SSCB) with solid state commutation; and,

c. 50A/400 VDC transistor-type power switch SSPC.

1.1 Project Synopsis (Continued)

Tasks VI and VII, ENGINEERING MODELS, produced prototype designs of the EM/SSCB and the transistor-type SSPC concepts. These were successfully tested according to formulated test plans with the transistor-type SSPC design demonstrating the capability of operation in a vacuum environment.

1.2 Accomplishments

The following is a list of significant program accomplishments:

a. Circuit technology has been develcped and demonstrated that establishes the technical feasibility of HVDC switchgear rated at 25 to 80A for applications at potentials from 200 VDC to 1100 VDC.

b. Critical HV semiconductor devices have been selected and successfully utilized that meet the stress of HV/high power load control.

c. Three innovative switchgear designs have been developed utilizing different HV/power switch elements that offer various advantages for system implementation.

d. Excellent operating efficiencies, in excess of 99.5%, were obtained that would enhance overall system efficiency and reduce SSPC heat sinking requirements.

e. A total of seven packaged brassboards and prototype units were successfully environmentally tested for varied and diverse loads, voltage variations, and transient conditions that verify the SSPC capability to operate under conditions encountered in system application.

1.2 Accomplishments (Continued)

f. The success of vacuum tests verified the capability of HVDC SSPC operation in this environment.

g. Performance specifications for the three HVDC SSPC versions are included as an appendix to this report.

1.3 Conclusions and Recommendations

This program has demonstrated the technology readiness of HVDC SSPC's with current ratings of up to 80A in the range of 200 VDC to 1100 VDC. The successful development of the three types of HVDC switchgear offers the user options that can result in optimization to a given application. Table 1-1 is a matrix of important parametric considerations for the three designs. One capability that was not included is vacuum operation, for which the transistor-type SSPC was successfully vacuum tested and the other two types are also compatible. For this application, the EM/SSCB hybrid device would require hermetic sealing and other considerations which Westinghouse and others have already demonstrated in numerous high altitude/space circuit designs.

1.3 Conclusions and Recommendations (Continued)

A recommendation concerning the SSPC packaging design is a result of the vacuum test of the 50A/300 VDC SSPC: the 95°C temperature rise of the power switch transistors required the SSPC mounting plate temperature to be maintained at 10°C maximum for reliable operation (based on AS-4613, Class A, Reliability Criteria). Thermal conduction efficiency can be improved by using an integral base-heat sink design and polished finishes on the SSPC base and mounting surfaces (see Paragraph 9.4.3 on Page 9-26). This will result in a 50°C maximum mounting plate temperature for reliable operation - a significant improvement. This type of construction is recommended for high power SSPC's.

Table 1-1

HVDC Switchgear Matrix

Parameter	SCR-Type	EM/SSCB	Transtr.-Type	Units
Power Switch Configuration	SP-NO	SP-Latch	SP-NO	-
Voltage	500-1100	200-400	200-400	VDC
Current	25	80	50	ADC
Overload Protection	Yes	No	Yes	-
Short Circuit Protection	No	No	Yes	-
Switch Drop/Efficiency	2	1	3	*
Size/Weight	3	1	2	*

*Numerical values are in order of desirability.

1.3 Conclusions and Recommendations (Continued)

The following recommendations are made for further HVDC SSPC developments:

1. The EM/SSCB effort demonstrated the feasibility of this concept for HVDC load switching. The advantages of not requiring standby load power and having low contact drop are desirable in many applications. Further effort is recommended to increase power rating (operating voltage particularly) and to provide a completely solid state commutation circuit.
2. The power switch for the transistor-type HVDC SSPC utilizes a complimentary PNP-NPN Darlington power stage which has been advantageously used for 120 VDC and 270 VDC SSPC's. The 400 VDC application appears to be a limit, at least for the present, because of the PNP power transistor technology. The NPN and PNP transistors used were rated at 500-550 VCEO; the soon to be available NPN bipolar and N-Channel Field Effect power devices in excess of 1000 VDC ratings warrants their evaluation for switching applications and at HVDC potentials, especially above 400 VDC. Also, a hybrid Darlington power stage consisting of a FET driving a bipolar should be evaluated for improving power gain, size, weight, and current ratings.

1.3 Conclusions and Recommendations (Continued)

3. Currently, there is considerable effort in developing gate turn-off thyristors (GTO) and ratings of up to 600A/1600V are available. For applications above 25 KW and 1000 VDC and higher, GTO power switch development and evaluation is recommended to provide significant commutation circuit size reductions.

SECTION II

INTRODUCTION

2.1 Background

Analysis of future near Earth Energy needs has identified a variety of missions in spacecraft configurations requiring significant increases in electrical power beyond the ten kilowatt level. In seeking to extend Space Shuttle capabilities and to establish low cost semi-permanent space stations in near Earth, several electrical components, circuit control techniques, and power distribution systems are required to provide a technology base for future space systems in the multi-KW to megawatt power levels.

Recent space station studies have identified high voltage DC power control equipment as a specific technology that requires development. At the 270/300 VDC level, switchgear is under development for both distribution busses and spacecraft loads for the 25 to 100 KW power levels appropriate for near term space power systems such as Space Construction Bases and Large Power Modules.

Above 100 KW, the experience of utility power companies indicates that voltages of up to 1 kilovolt may be required for power distribution and transmission over extended distances on large base power generation and manufacturing bases. This program is directed to determine feasibility of high voltage switchgear capable of controlling 25 KW of electrical power.

2.2 Objectives

Originally, the objective of this program was to develop one kilovolt-level switchgear modules for 25 KW distribution applications. Analytical study, experimental analysis, and breadboard evaluation were to be used to develop and demonstrate switchgear concepts and feasibility.

Nine months into the program, in September, 1979, the program was amended to extend the operating voltage range from 500-1100 VDC to 200-1100 VDC. Based upon subsequent evaluations, engineering models were to be designed, fabricated, and evaluated that would be capable of operation in a vacuum.

2.3 Outline of Tasks

To accomplish these objectives the program was divided into seven tasks as follows. Originally, the program consisted of three technical tasks which were amended upon the completion of Tasks I and II to increase the scope of Task III and to add Tasks IV through VII.

Task I - Preliminary Analysis

Task I - Trade-Off Studies

Task III - Switchgear Design Evaluation and Analysis

Task IV - Design and Fabrication

Task V - Breadboard Test and Evaluation

Task VI - Engineering Modules; Design and Fabrication

Task VII - Test and Evaluation

2.4 Specifications for HVDC Switchgear

	Parameter	Type A	Type B
a.	Rated Operating Voltage	1000 ± 100 VDC	300 ± 100 VDC
b.	Operating Voltage Range	500-1100 VDC	200-400 VDC
c.	Output Current	25 Amperes	80 Amperes
d.	Control Voltage	28 ± 7 VDC	28 ± 7 VDC
e.	Turn-On Voltage	3 ± 1 VDC	3 ± 1 VDC
f.	Turn-Off Voltage	3 ± 1 VDC	3 ± 1 VDC
g.	Turn-On Time	0.01 to 10 msec.	0.01 to 10 msec.
h.	Turn-Off Time	0.01 to 10 msec.	0.01 to 10 msec.
i.	Max. Volt Drop @ Rated Load	3.0 VDC	0.2 VDC
j.	Power Dissipation ON Max.	250 Watts	20 Watts
k.	Power Dissipation OFF Max.	3 Watts	0.2 Watts
l.	Power Dissipation TRIP, Max.	25 Watts	-
m.	Efficiency @ Rated Load, Min.	99%	99%
n.	Control Current	10 ma.	10 ma.
o.	Load Current, Min.	0 @ Rated Voltage	0 @ Rated Voltage
p.	Fault Response Time	3 μsec.	3 μsec.
q.	Operating Temperature	40 to 100°C	40 to 100°C
r.	Operating Environment	Typical Vacuum and Zero "g"	
s.	Non-Operating Survivability	Typical Spacecraft Launch Shock and Vibration	

SECTION III

PRELIMINARY ANALYSIS (TASK I)

3.1 Task Objectives

a. Investigate and evaluate high voltage switching devices such as contactors, relays, semiconductors, and current limiters to identify the most qualified single device or combination of devices as the main switching elements of the HVDC switchgear.

b. Assume power sources for analysis and circuit simulation will be solar cell arrays or a DC-DC inverter of the "bridge" or "series-resonant" type.

c. Consider load control and compatibility including resistance, inductance, capacitance, and motor load characteristics.

d. Define switchgear models and/or circuit concepts to accomplish the specified switching and protection functions.

3.2 Task Realignment

Early in this task, the objectives were redefined and modified to provide a direction and alignment with NASA's plans and objectives. These changes were as follows:

a. Assume a 1000V/25A solar array power source with 50A maximum fault current capability for SSCB interrupting and commutation considerations

3.2 Task Realignment (Continued)

b. Eliminate the proposed evaluation of a transistor power switch as the availability of adequate HV power transistors for this application was too far out in the future. This allowed program effort to be focused on the two most feasible candidates, the electro-mechanical-SCR, and the total SCR power switch versions.

c. Delete the plan to develop a 1 KV input, 28 VDC output, power supply in favor of utilizing a 28 VDC control signal. This has the advantage of enabling the SSCB to function as an electrically-held relay or breaker as well as allowing more effort to be spent on the basic development problem, HVDC power switching.

d. Evaluate the need for overload protection - the advantage of circuit simplicity in the SSCB would be traded off against SSCB continuous overload capability and the system consequences of continuous overload flow.

3.3 SCR-Commutated Power Switch Description

The electro-mechanical and SCR power switches were selected as the most feasible upon the basis of capability to perform HVDC load switching and upon the availability of the necessary components. Both approaches utilize solid state controlled commutation: the electro-mechanical power switch requires commutation to preclude contact burning while the SCR power switch requires forced commutation to achieve current interruption.

Figure 3-1 depicts a simplified HVDC power switch circuit with SCR commutation. This circuit diagram applies to both the electro-mechanical and SCR versions with the exception that the contact arc sensing circuit is not required for the SCR-type power switch element.

3.3.1 Performance Scenario

Referring to Figure 3-1, assume that the power switch is an electro-mechanical contactor, is closed and carrying load current. When the power contact is opened by a trip signal, the arc detection circuit senses contact opening and "signals" the commutation firing circuit to initiate commutation by providing gate signals to SCR1 and SCR2. The conduction of SCR1 and SCR2 causes the removal of load current from the power switch for a brief period of time, determined by the values of L, C, VDC, and IL. This allows the power switch to change to the nonconductive, voltage blocking state. The function of the recharge circuit is to maintain an adequate charge in commutation Capacitor C, to assure power switch turn-off.

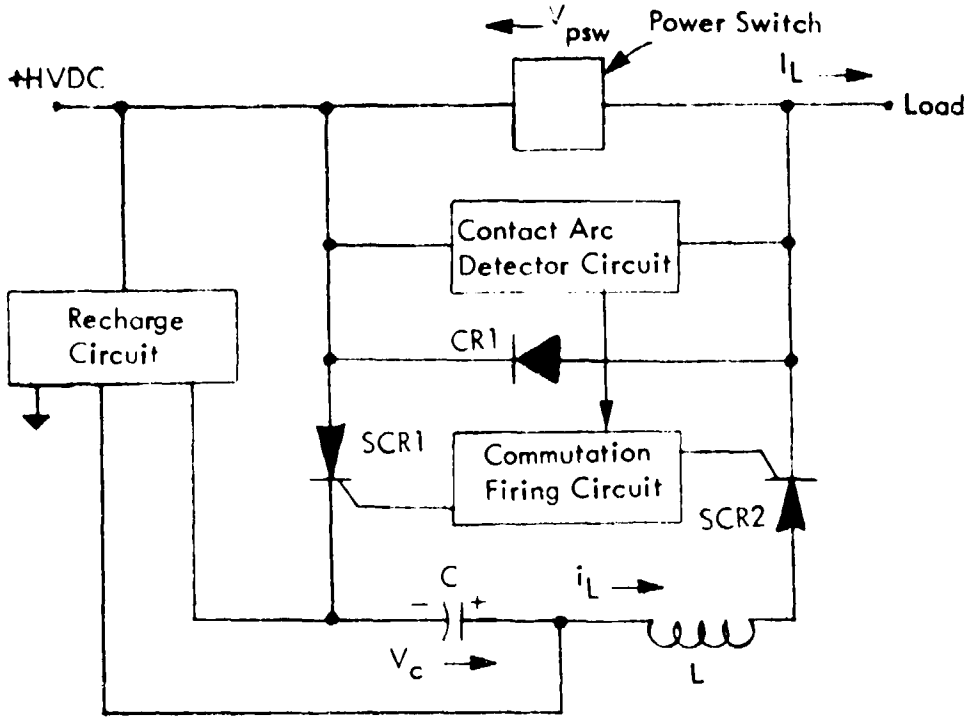


Figure 3-1

HVDC Power Switch Circuit Diagram With SCR Commutation

3.3.1 Circuit Operation

Referring to Figures 3-1 and 3-2, assume that Capacitor C has been charged to the V source potential of the polarity shown prior to the power switch contact opening. SCR1 and SCR2 effectively isolate C from source, power switch, and load to assure successful commutation operations. When the contact opens, an arc is sensed by the contact arc detection circuit, initiating a short time delay to allow the contacts to get separated an amount sufficient to guarantee the arc will not reignite when extinguished. When the time delay is complete, commutation is initiated by the commutation firing circuit which sends current pulses to SCR1 and SCR2 gates simultaneously, causing them to conduct. The commutation "tank" composed of C and L functions to provide a half-cycle sinusoid of current through SCR1, SCR2, and diode CR1. When the current reaches the load current magnitude, the power switch contact current is zero. The arc extinguishes and the contact voltage is zero. Commutation current in excess of load current goes through diode CR1, limiting the load voltage to supply voltage potential. The load current is supplied through the commutation circuit until the commutation current is below the load current level. When this occurs, the contact voltage reappears and the load is shut off at the rate controlled by the sinusoidal current. At the completion of commutation, C is charged to line potential in the opposite polarity as shown in Figure 3-2a.

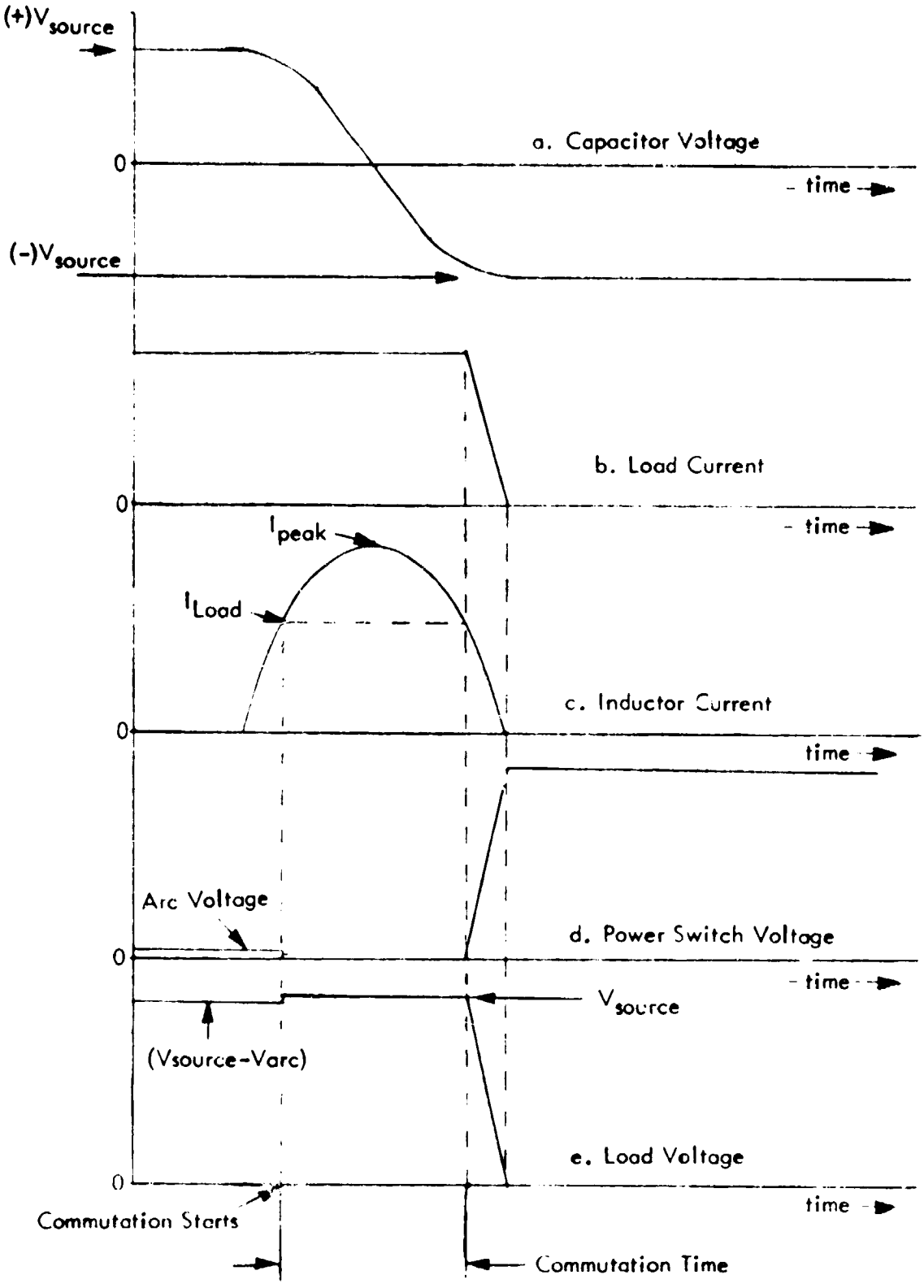


Figure 3-2

HVDC Power Switch Commutation Waveforms

3.3.1 Circuit Operation (Continued)

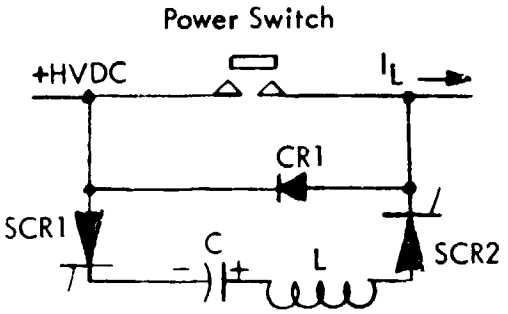
To reset the commutation circuit for the power switch turn-off, Capacitor C must be discharged and recharged to the value it was before commutation: a voltage swing of two times V source; this is accomplished by the recharge circuit. An inhibiting signal provided by the logic circuit (not shown) to the commutation firing circuit precludes a subsequent commutation operation until Capacitor C is sufficiently recharged.

3.4 Power Switch Commutation Analysis

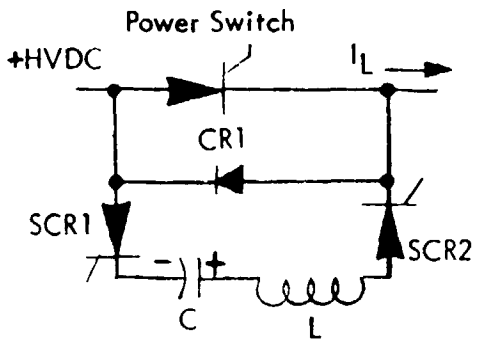
3.4.1 Design Specification

For this analysis, the following design specifications result from operational and component requirements:

Operating Voltage Range	500-1100 VDC
Rated Load Current	25A
Maximum Fault Current	50A
Power Switch Element	Electro-Mechanical or SCR Type (Figure 3-3)
Minimum Commutation Time	75 μseconds



a. Electro-Mechanical Commutation Circuit



b. SCR Commutation Circuit

Figure 3-3

Power Switch Commutation Circuits

3.4.2 Determination of C and L Values

As shown in Figures 3-2 and 3-4, the commutation current pulse is a sinusoidal half-cycle waveform. Significant waveform variables are:

t_c - Commutation Pulse Duration Time

t_{off} - Power Switch Off Time

I_f - Fault Current Level

I_p - Peak Pulse Current

The value of C can be determined at its worst case condition when at minimum supply voltage, C must supply the maximum value of fault current to the load. Since for a capacitor:

$$e_c = (i_c/C)(dt)$$

or $$C \approx (Ic/\Delta Ec)(\Delta t)$$

and at 50A, 500V, and 75 μseconds:

$$C \approx (50/500)(75 \times 10^{-6}) = 7.5\ \mu F. \qquad (1)$$

To determine the value of L, an ideal series resonant LC-circuit is assumed and a value of 45° is selected for θ to provide a ratio of I_f/I_p of .7. Then, using the inductive relationship

$$e_L = L(di/dt)$$

or $$L \approx \Delta\, e_L(\Delta t/\Delta iL)$$

and evaluating for $\Delta T = t_{off}/2$, $\Delta e_L = 500$, and $\Delta iL = 50$,

and $$L \approx 500(75/2)(10^{-6})/50 = 375\ \mu H. \qquad (2)$$

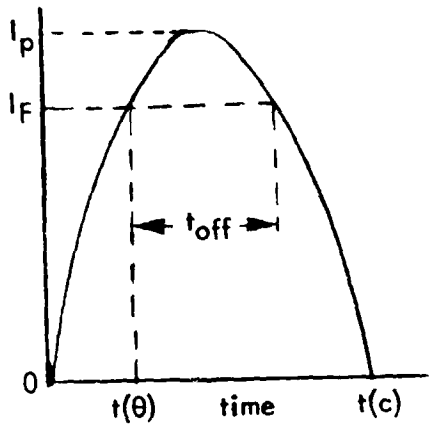


Figure 3-4

Commutation Current Pulse

3.4.2 Determination of C and L Values (Continued)

For the values of C and L derived in Equations (1) and (2), the following operating times will be obtained.

$t_c = (1/2)/f_{LC} = (1/2)(2\pi\sqrt{(375)(7.5)})(10^{-6}) = 167$ μsec.

$f_{LC} = 3$ KHz

$t_{off} = (167/2)(10^{-6}) = 83$ μsec. (3)

For commutation at 500V, 50A:

$$I_p = \sqrt{(C/L)}(VDC)^*$$

or $$I_p = \sqrt{(7.5/375)}(500) = 71A, \quad (4)$$

and for commutation at 1100 VDC:

$$I_f \text{ (Max.)} = (C)(VDC)/t_{off}$$

or $$I_f \text{ (Max.)} = (7.5)(1100)/(75) = 110A,$$

also $$I_p \approx 110/\sin 45^\circ = 156A.$$

*This expression is derived from stored energy relationships.

3.4.2 Determination of C and L Values (Continued)

Thus, at 1100 volts, the commutation circuit is capable of clearing fault currents of 110A or 2.2 times that at 500 volts since this ability is proportional to the supply voltage level.

The commutation C and L components, then, should have the following minimum characteristics:

$C = 7.5\ \mu F/1100\ VAC,$

$L = 375\ \mu H/1100\ VAC,$

and be capable of operation with a 156A, 167 μsecond current pulse.

3.4.3 Special Conditions

3.4.3.1 Power Switch Reverse Bias

The SCR power switch requires reverse bias voltage for shut-off, about 50 volts for 30 μseconds being desirable for the Westinghouse Type 507 devices that are to be used. In Figure 3-5, L1 is placed in series with CR1 to provide this reverse bias voltage; however, L1 causes undesirable voltage transients that affect both source and load that must be considered.

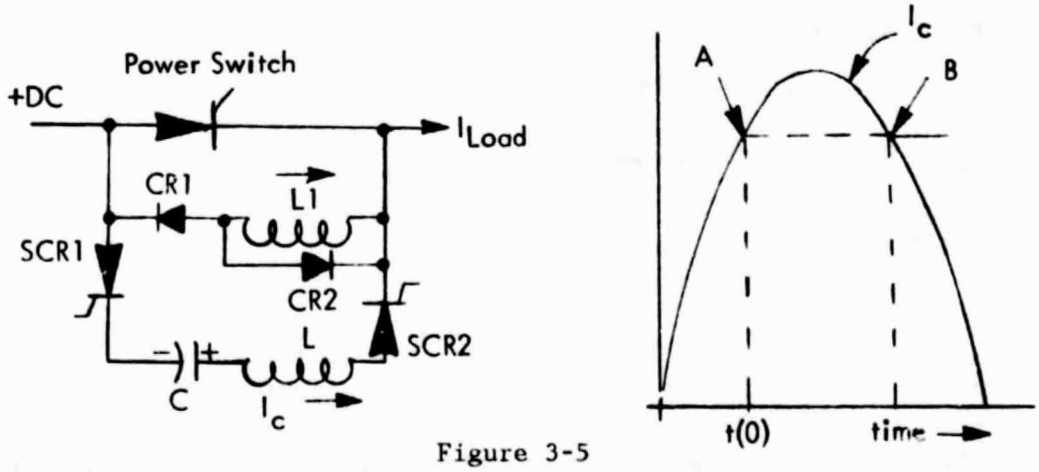


Figure 3-5

Reverse Bias Circuit

3.4.3.1 Power Switch Reverse Bias (Continued)

In Figure 3-5a, when commutation is initiated, the current I_c begins to increase at the rate set by L and C. When $I_c = I_{load}$ (Point A), the capacitor still has extra energy which it will put into the system. In order to generate a reverse bias voltage (under short circuit load), the source must see reverse polarity voltage. The amount of reverse voltage is set by the inductor L1 and components C and L.

To determine the value of L1, it is assumed that L1$\ll$L and the relationship used is

$$e_{L1} = L1(di/dt) \qquad (1)$$

which in the worse condition must provide power switch reverse bias voltage for

$$I_{Load} = 50A \text{ at } 500 \text{ VDC}.$$

Using the C and L values determined in the previous section, rearranging Equation (1) and evaluating L1 at t = t (θ):

L1 (Min.) = 50/(di/dt) = (50V)/(d(70 SIN $2\pi f_{LC}$)/dt), and

L1 (Min.) = (50V)/(70) (2π) (3,000) Cos (45^0) = 54 μH.

L1 then will be required to support at least 50 volts for 30 μseconds to assure commutation; however, it will provide a greater reverse voltage transient at turn-off with a 1100V supply and a 156A load and this transient voltage will appear across the load in addition to 1100 volts:

E_{L1} (Max.) = (54 μH)(156)(2π)(3,000)(.707),

E_{L1} (Max.) = 112 volts,

3.4.3.1 Power Switch Reverse Bias (Continued)

and E_{load} (peak) = 1100 + 112 = 1212 volts.

Referring to Figure 3-5, Diode CR2 is used to commutate L1 when its di/dt is of negative value. Consequentially, L1 is precluded from forward biasing the power switch when the current slope begins to decrease and I_p is passed.

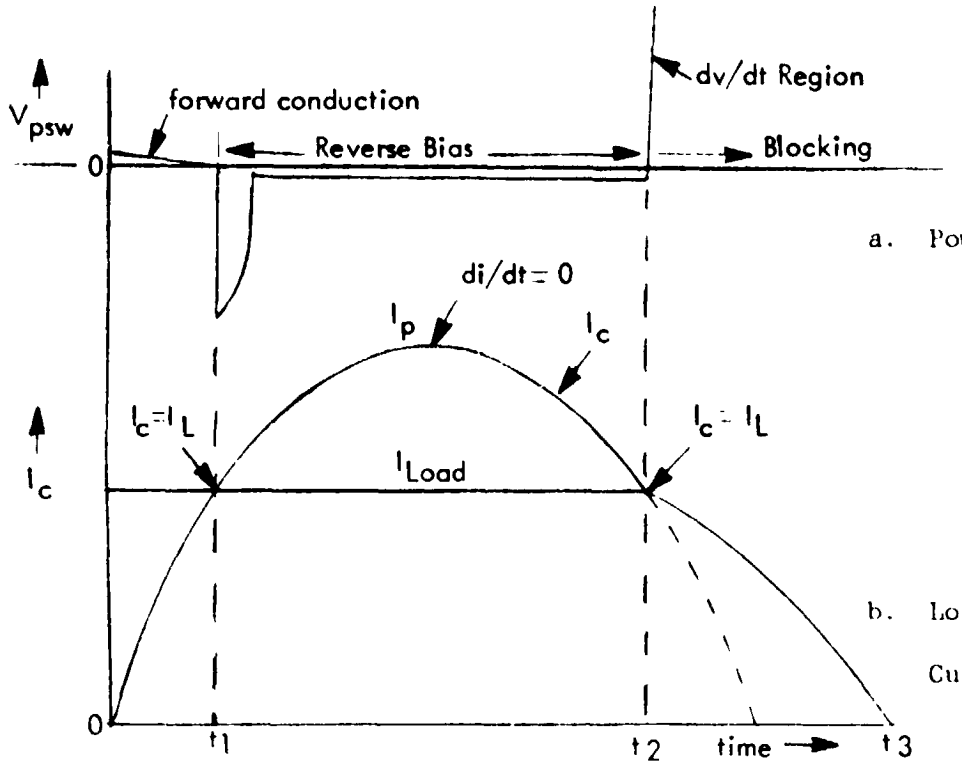
Figure 3-6a depicts the commutation voltage across the power switch, SCR3, with the addition of L1, assuming that L1 does not saturate. In the reverse biasing interval, extending from t_1 to t_2, the power switch is impressed with reverse voltage first by the L1 induced voltage and then by the CR1 and CR2 conduction voltages.

When the value of I_c decreases below the I_L level after t_2, the rate of change of the SCR3 power switch blocking voltage, dv/dt, is critical and of concern. The current waveform in the interval from t_2 to t_3 is modified by the addition of load inductance L_L. The worst case commutation condition will be in opening a 156A/1100V circuit. From the power switch circuit, Figure 3-6c, the power switch voltage during this time interval will be

$$V_{psw} = VDC + I_L \cdot R_L + L_L(di_L/dt).$$

By differentiating this equation, utilizing the circuit values from Paragraph 3.4.2 and an L/R of 10^{-4}*, a dv/dt of 15V/μsecond is obtained which is well within the capabilities of SCRs, like the Westinghouse Type 507, that can be used for this application.

*Typical for resistance heaters.



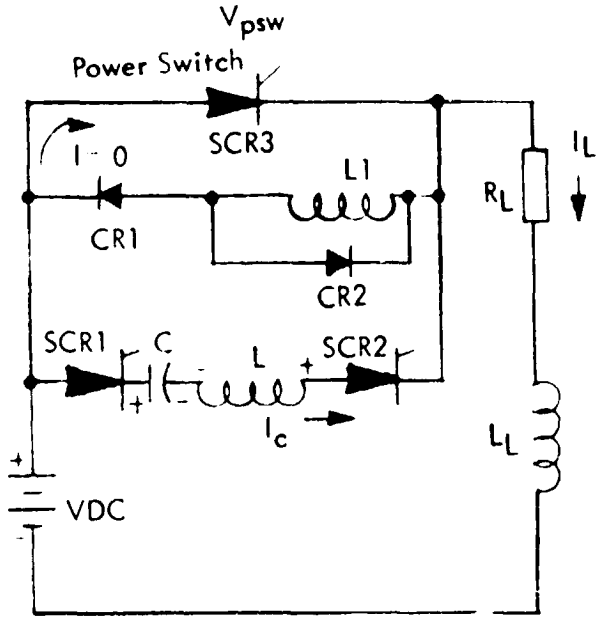


Figure 3-6

Power Switch Commutation Waveforms

3.4.2 Snubber Considerations

Considering the benign value of dv/dt calculated for the power switch, a snubber circuit for the power switch would not appear necessary. However, the non-ideal recoveries of power switch semiconductors caused by carrier storage times and circuit wiring inductances will cause high current, short duration transients that result in spike transient voltages. Since these transients and corresponding snubber design procedures are extremely difficult to analyze, the snubber R and C values will be determined by test evaluation. Figure 3-7 depicts the snubber circuit to be used. In this circuit, R_s limits the instantaneous current through SCR3 at turn-on, and at turn-off, C_s limits dv/dt and D_s limits the instantaneous voltage level.

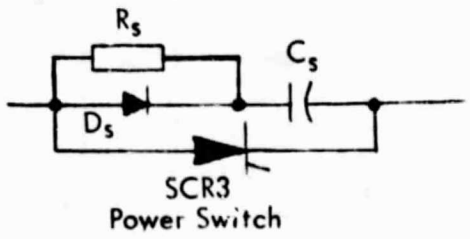


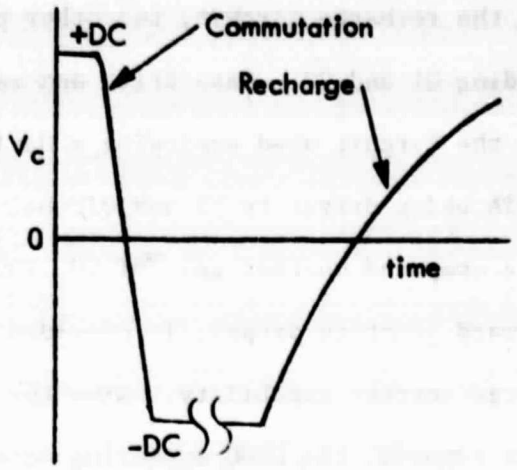
Figure 3-7

Snubber Circuit

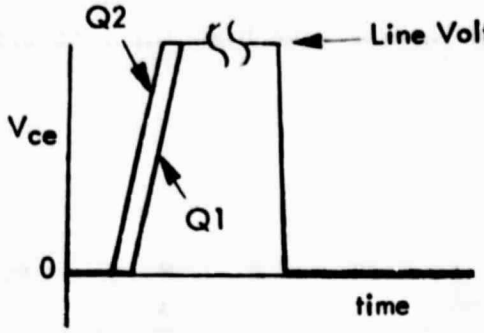
3.5 Recharge Circuit Analysis

In Figure 3-1, the recharge circuit is used to maintain the Capacitor C voltage at the HVDC supply level for providing commutation energy. Figure 3-8 shows the implementation of this circuit and voltage waveforms resulting from a power switch commutation. Notice that the recharge transistors, Q1 and Q2, have a high value of applied voltage only during the commutation interval and are in a conducting mode elsewise. Resistors R1 and R2 and Diodes CR1 through CR4 control and limit the recharge circuit voltages and currents.

After commutation is complete, the commutation capacitor has charged to a voltage in the reverse direction equal to the +DC supply voltage and must be recharged. The recharge transistors must handle the voltage and current to turn the capacitor voltage around for another cycle. For this application, the Motorola Type MJ12005, 1500 Vceo transistor, was selected on the basis of voltage and Safe Operating Area ratings.



a. Capacitor Voltage



b. Q1 and Q2 Voltage

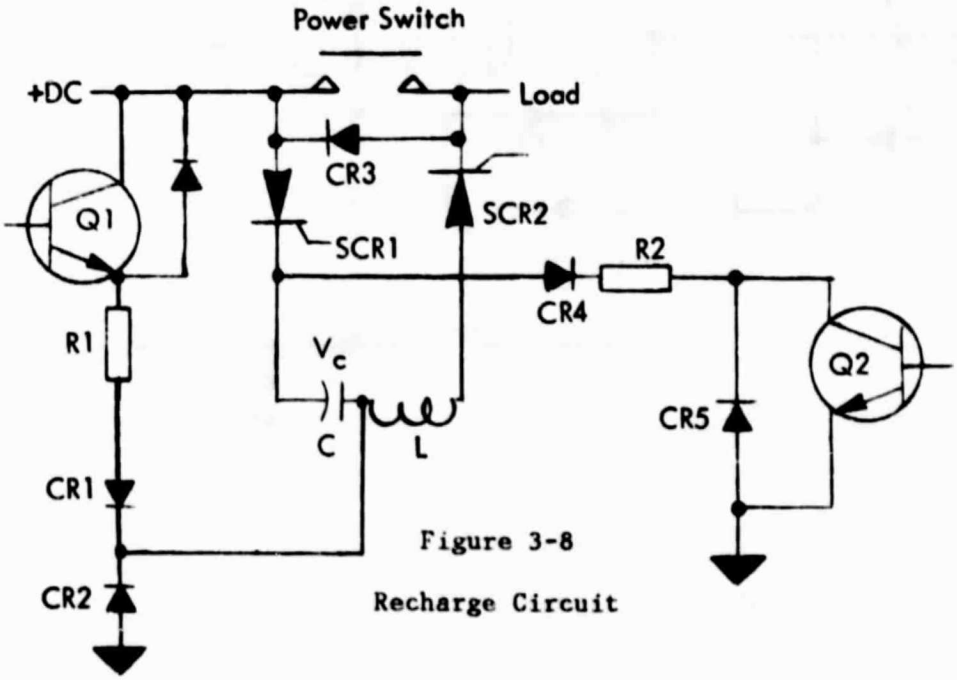


Figure 3-8

Recharge Circuit

3.5 Recharge Circuit Analysis (Continued)

In designing the recharge circuit, two other parameters were considered regarding Q1 and Q2: base drive and reverse biasing. Figure 3-9 shows the circuit used employing a Darlington configuration, Q1A being driven by T1 and Q1B being current coupled from Q1A. With a compound current gain of 50, 100 ma drive at 2.1 volts (three forward junction drops), is provided for Q1A-Q1B to provide 5A recharge current capability. When the base drive signal to Q1A and Q1B is removed, the HVDC appearing across the collectors results in a small current flow through R1, R2, and CR1 (6.8 volt Zener) that provides reverse base bias for both Q1A and Q1B via R3.

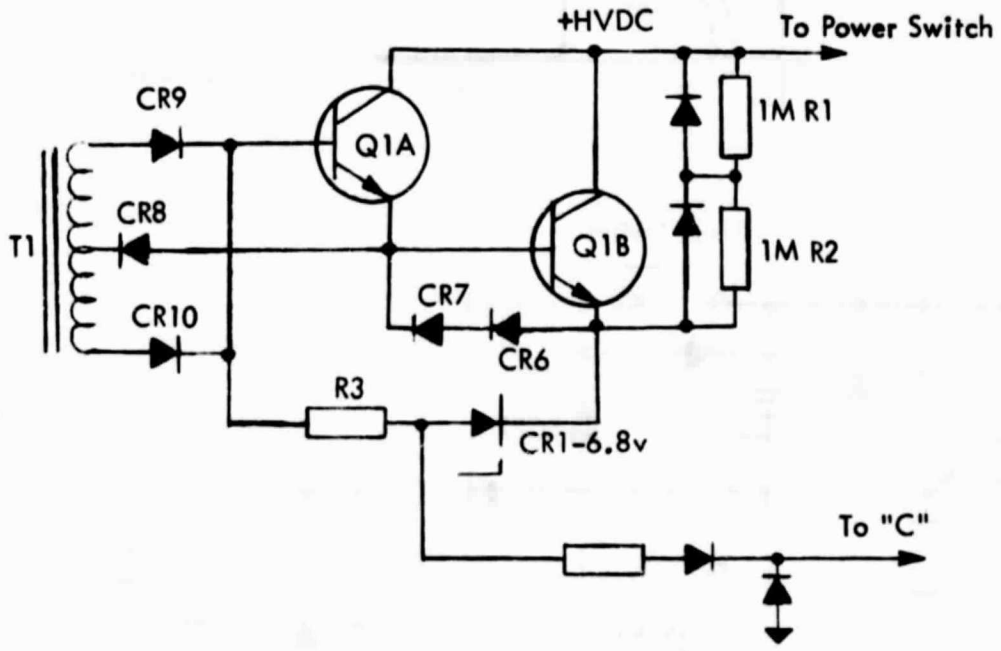


Figure 3-9

Recharge Transistor Circuit

3.6 Control, Logic, and Protection Requirements

From the analyses of the HVDC Breaker circuit with its commutation and recharge circuit elements, definition was completed for the control, logic, and protection portions of the development. In summary, these are:

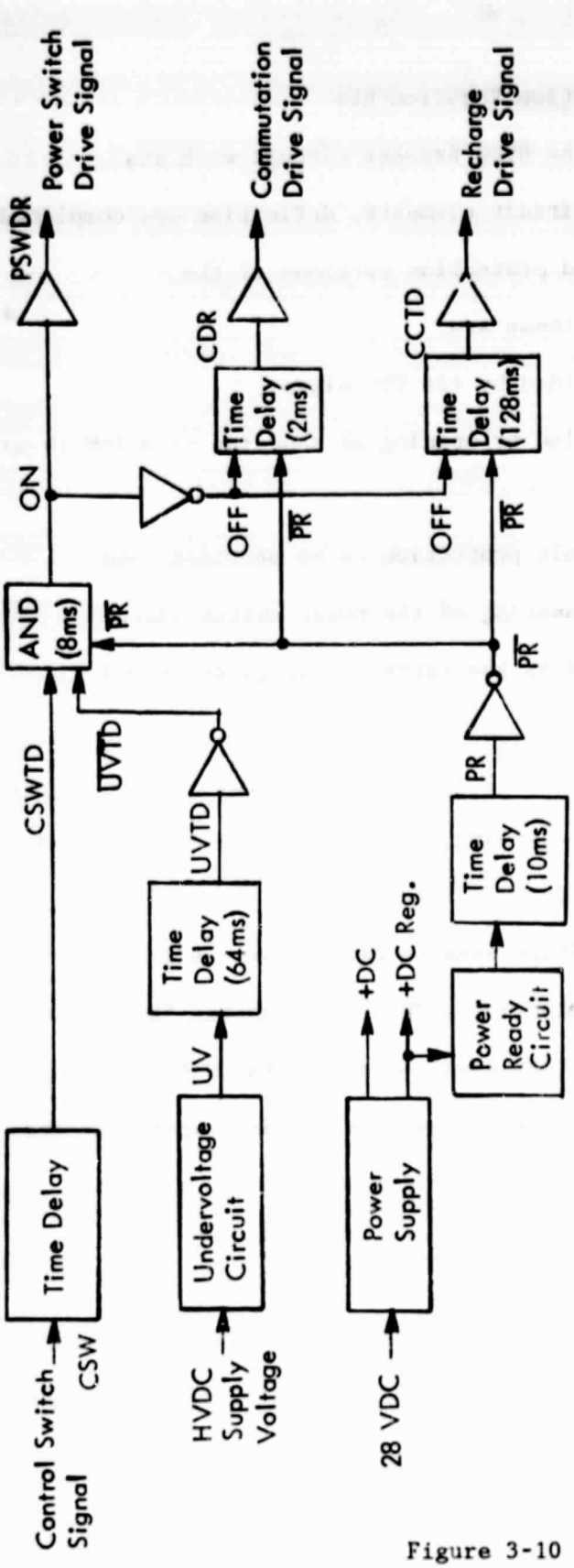
a. control power provided by +28 VDC signal;

b. SSCB to be controlled by opening or shorting of a 10V/10 ma signal;

c. either UV or OC fault protection to be provided; and

d. the timing and sequencing of the power switch control signals as required by the circuit configuration and circuit parameters.

Truth Table 3-1, Functional Diagram Figure 3-10, and the Figure 3-11 oscillograms depict the timing, sequencing, and operation of the control, logic, and protection signals. For this particular implementation, an undervoltage sensing circuit was utilized to provide system overload protection. This utilized the "knee" characteristic of a solar array power source. The UVTD (.064 seconds) and operating level (approximately 500 VDC) were selected for source and system compatibility. A more complete circuit description will be provided in Section V, Paragraph 5.3.



Glossary

CCTD	Commutation Complete Time Delay
CDR	Commutation Drive
CSW	Control Switch
CSWTD	Control Switch Time Delay
PR	Power Ready
$\overline{PR}$	Power Ready "Not"
PSWDR	Power Switch Drive
RDR	Recharge Drive
UV	Undervoltage
UVTD	Undervoltage Time Delay

Figure 3-10

Functional Diagram for HVDC Power Switch Control Circuit

Table 3-1

Control Logic Truth Table For 1 KV/25A Power Switch Control Circuit

Condition	Control Switch Position	Logic Signals						Logic Output Signals		
		CSW	CSWTD	ON	UVTD	CCTD	CDTD	PSDR	CDR	RDR
1. Power Up With CSW Open:										
$0 < t < .012$	Open	0	0	0	0	0	0	0	0	0
$.012 < t < .140$	Open	0	0	0	0	0	1	0	1	0
$.140 < t < \infty$	Open	0	0	0	0	1	1	0	1	1
2. Power Up With CSW Closed:										
$0 < t < .018$	Closed	1	0	0	0	0	0	0	0	0
$.018 < t < \infty$	Closed	1	1	0	0	0	0	1	0	1
3. Control Switch Opened From "ON" Condition:										
$0 < t < .008$	Open	0	1	1	0	0	0	1	0	1
$.008 < t < .010$	Open	0	0	0	0	0	0	0	0	0
$.010 < t < .136$	Open	0	0	0	0	0	1	0	1	0
$.136 < t < \infty$	Open	0	0	0	0	1	1	0	1	1
4. Control Switch Closed:										
$0 < t < .008$	Closed	1	0	0	0	1	1	0	1	0
$.008 < t < \infty$	Closed	1	1	1	0	0	0	1	0	1
5. Undervoltage:										
$0 < t < .064$	Closed	1	1	1	0	0	0	1	0	1
$.064 < t < .066$	Closed	1	1	0	1	0	0	0	0	0
$.066 < t < .194$	Closed	1	1	0	1	0	1	0	1	0
$.194 < t < \infty$	Closed	1	1	0	1	1	1	0	1	1
6. Reset:										
$0 < t < .008$	Open	0	1	0	1	1	1	0	1	1
$.008 < t < \infty$	Open	0	0	0	0	1	1	0	1	1
7. Reclose: Same As Item 4										

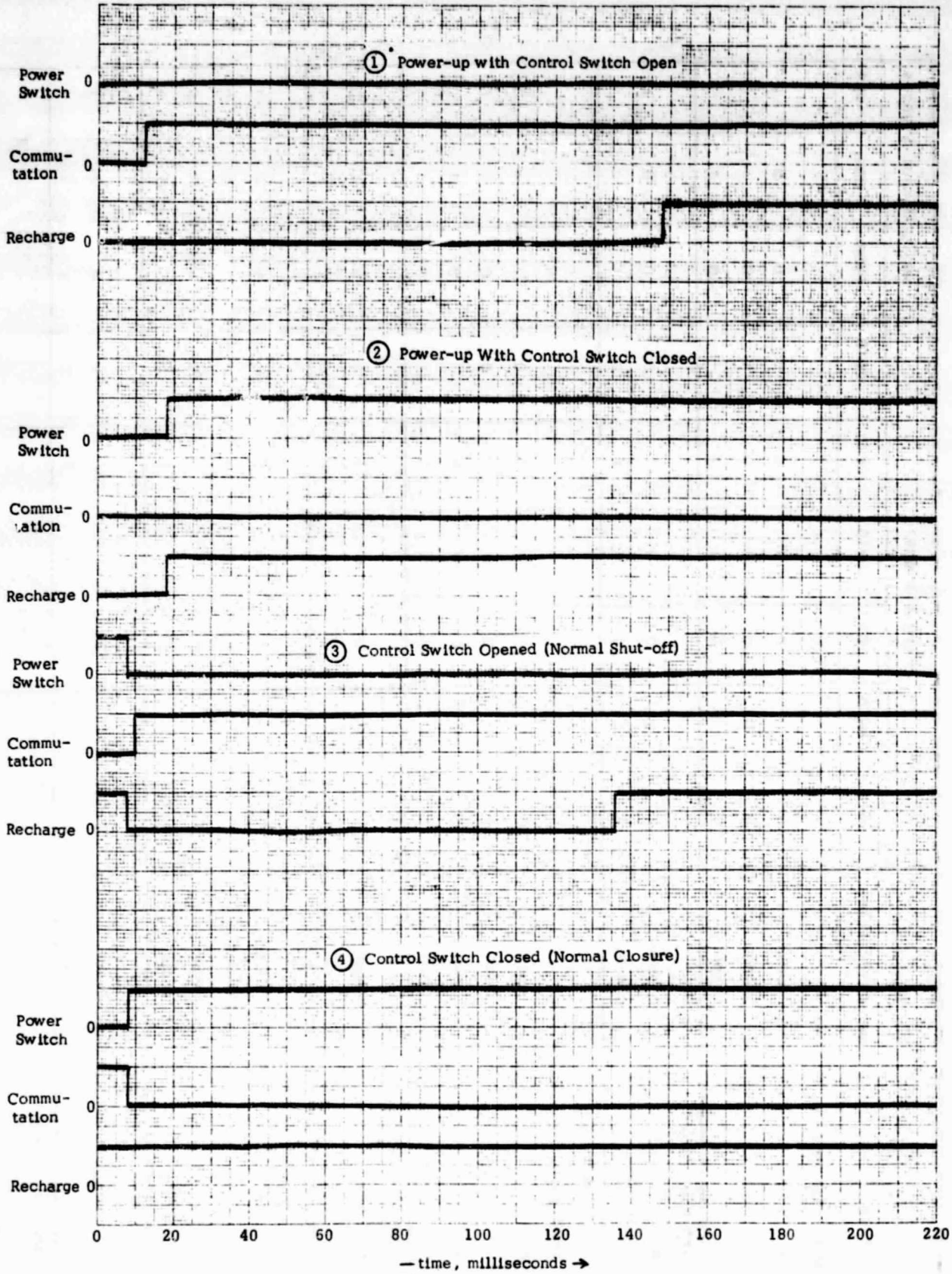


Figure 3-11

Control Logic Output Signals

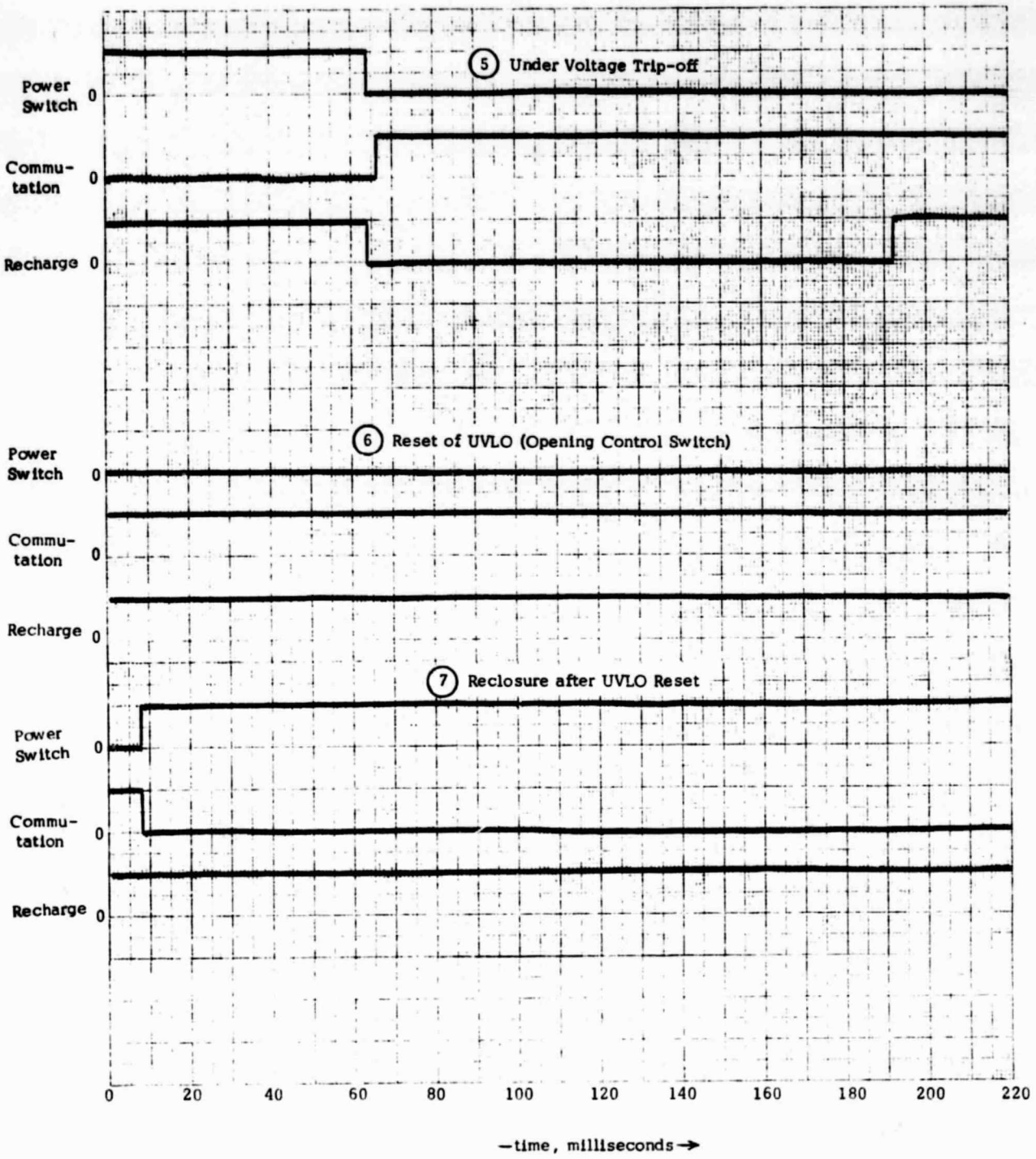


Figure 3-11

Control Logic Output Signals (Continued)

SECTION IV

TRADE-OFF STUDIES (TASK II)

4.1 Task Objectives

Using the switching and control concepts developed in Task I, a trade-off comparison was to be performed for the purpose of interactions between performance, physical size, cost, reliability, and related parameters. Results of this trade-off would be utilized for the Task III, Design Evaluations.

4.2 Results

A somewhat simplified tabulation of the Trade-Off Study appears in Table 4-1. This is a comparison of the electro-mechanical and SCR, 1 KV/25A power switches appearing on Page 3-4. From this comparison and considering the intended space applications, it was concluded that the SCR power switch version was the better choice. Consequently, the electro-mechanical version was placed in a backup role and focus placed on the SCR power switch.

Table 4-1

Power Switch Performance Comparison

Item	Electro-Mechanical	SCR	Remarks
Voltage Drop at 25A	.3-.4 Volts	.9 Volts	
Life	50K Operation	Unlimited	A reasonable breaker life expectancy is for 50K operations with eventual increasing contact voltage drop degradation.
Close Time/Trip Time	30 msec./15 msec.	Limited By Noise Immunity Circuits	Breaker close-time is determined by the mechanism dynamics and coil inductance; both minimum close and trip-times are directly related to the physical size.
Reliability Predictions	79K Hours MTBF	246K Hours MTBF	Based on 50°C operation, ground fixed ambient MIL-HBK-217C.
Hazardous Failure Mode	See Remarks	See Remarks	The breaker has a hazardous failure mode if the commutation circuit should fail: contact arcing will destroy the breaker and possibly cause a fire. This hazard does not exist for the SCR power switch which will remain conducting with a commutation failure.
Control Circuits	See Remarks	See Remarks	The arc voltage of the breaker must be sensed for shut-off. This requires either a special set of matched resistors or a circuit referenced to the positive line. In any event, the requirement coupled with the above failure mode requires an isolated DC supply be generated in addition to the normal 28 volt control input. The SCR control circuits can all be referenced to ground with a single supply.
Power Switch Dissipation At 25A	14 Watts	26.5 Watts	
Size ($In.^3$ /CC) Weight (Lbs./Kg.)	340/5570 8.5/3.9	300/4900 6.5/2.9	These size and weight estimates include the power switch and commutation components, but not associated connectors, control/drive circuitry, enclosure, etc.
Switch Cost	$800.00	$450.00	These estimates are based on small quantity costs for the power switch and commutation circuit components.

SECTION V

SWITCHGEAR EVALUATION (TASK III)

5.1 Task Objectives

a. Experimentally verify and demonstrate the switchgear concepts and switching techniques identified and defined in Tasks I and II.

b. Evaluate and summarize test data to provide one or two switchgear approaches and provide baseline design(s) compatible with the specifications.

5.2 SSPC Description

The circuit data developed during the program is shown and described on the following pages. In all, three units were built and tested; one "two dimensional" development breadboard plus two packaged breadboard units which are illustrated in Figures 5-1 and 5-2. The packaged units differ from the development unit in that overcurrent protection was provided in addition to undervoltage protection to provide a better means of overload. Also, fusing was provided to assure fault clearing at potentials below 500 VDC.

5.2 SSPC Description (Continued)

Included in Appendix A-1 is a design specification which defines performance parameters and packaging dimensions for this SSPC. The Westinghouse designated type number for this unit is AVC-45. Briefiy, it can be described as having an operating voltage of 500-1100 VDC with a current rating of 25 amperes. It is configured as a SPST-NO switch with an SCR as the switching device. It employs separately powered control logic circuitry for ON-OFF functions, fault protection, and status indication.

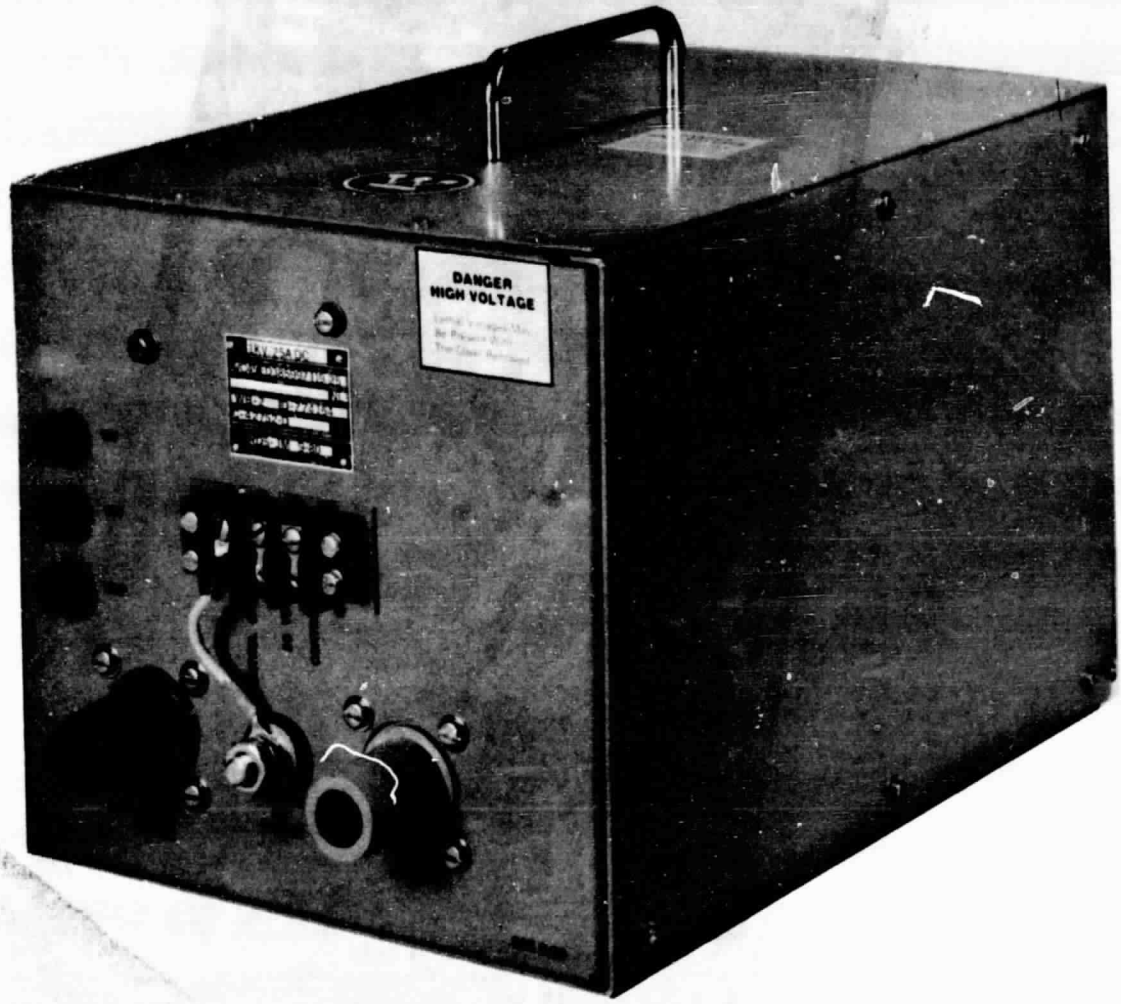


Figure 5-1

Type AVC-45 1 KV/25A SSPC

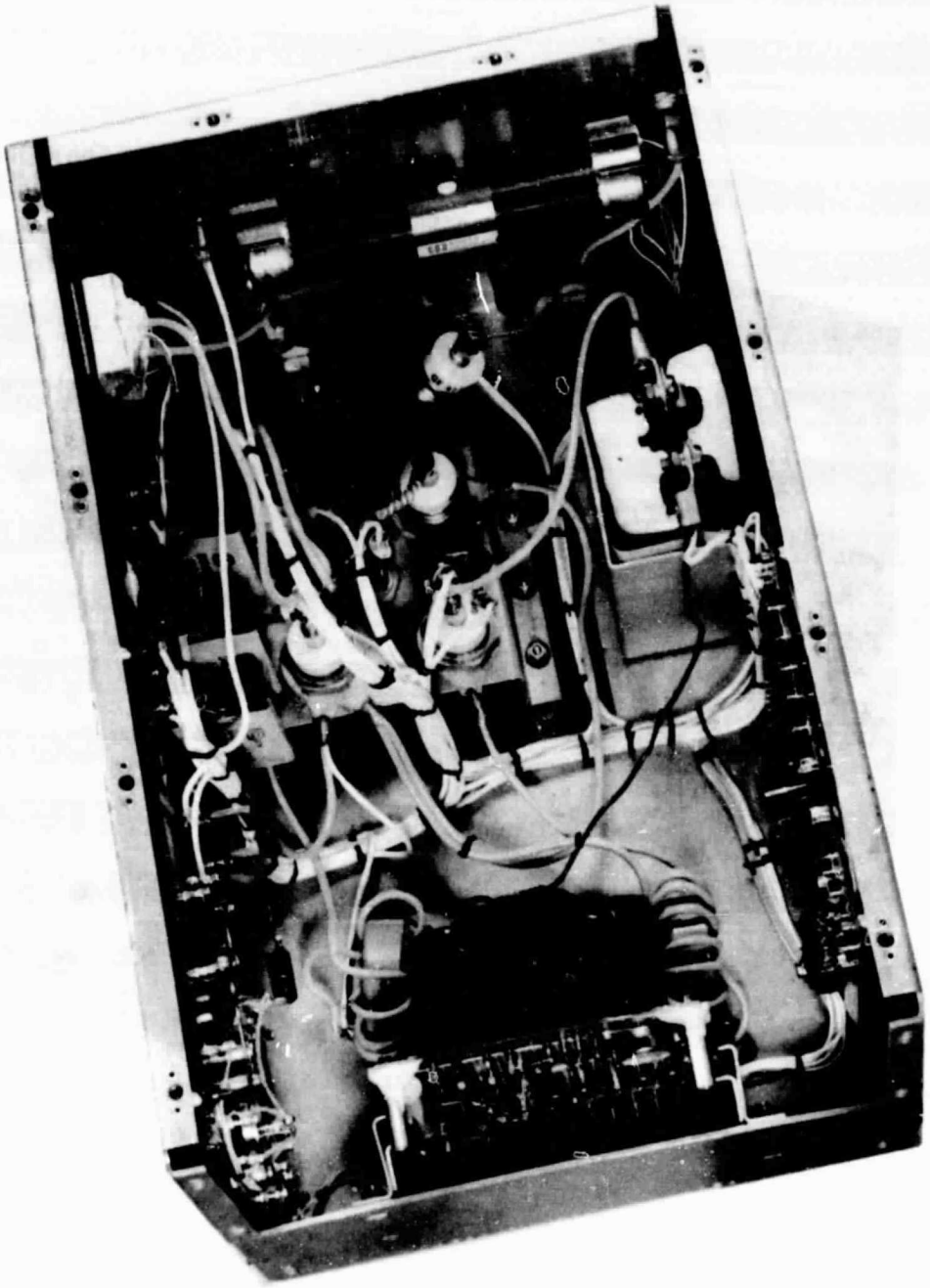


Figure 5-2

Type AVC-45 Internal View

5.3 Circuit Description

The schematic diagram for the AVC-45 SSPC is shown in Figure 5-3, and the associated legend in Table 5-1. A summary of the SSPC functions are as follows:

1. Control Functions
   a. Control Power Supply
   b. Control Switch Time Delay
   c. Power Ready
   d. Trip Lockout
   e. Power Switch Drive
   f. Power Switch
   g. Commutation Drive and Time Delay
   h. Recharge Drive and Commutation Complete Time Delay
   i. Clock
2. Protective Functions
   a. Overcurrent
   b. 28 VDC Low Voltage
   c. Power Undervoltage
3. Indication Function
   a. ON, OFF, TRIP Indication

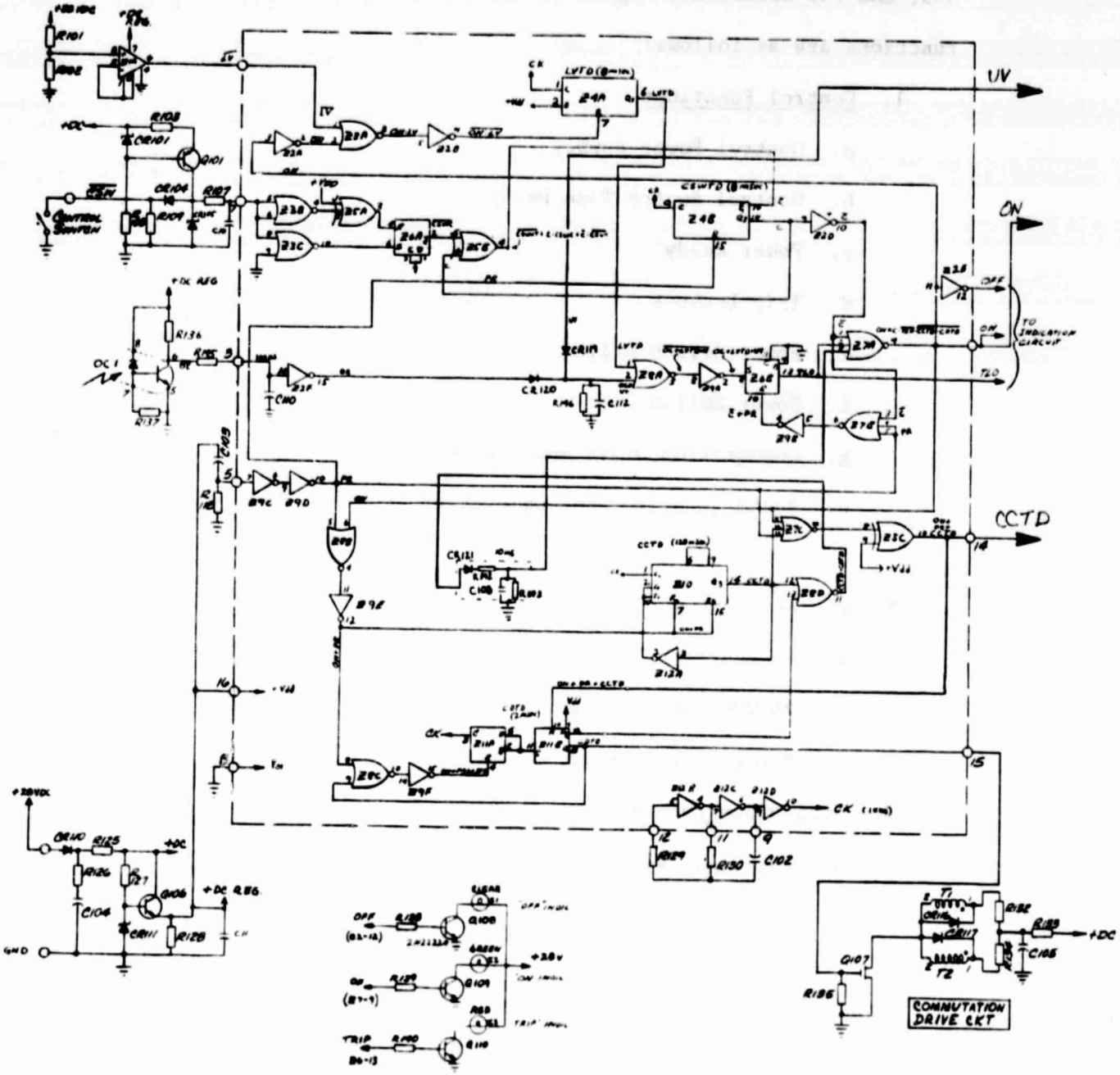


Figure 5-3

1 KV/25A DC SSPC Schematic Diagram

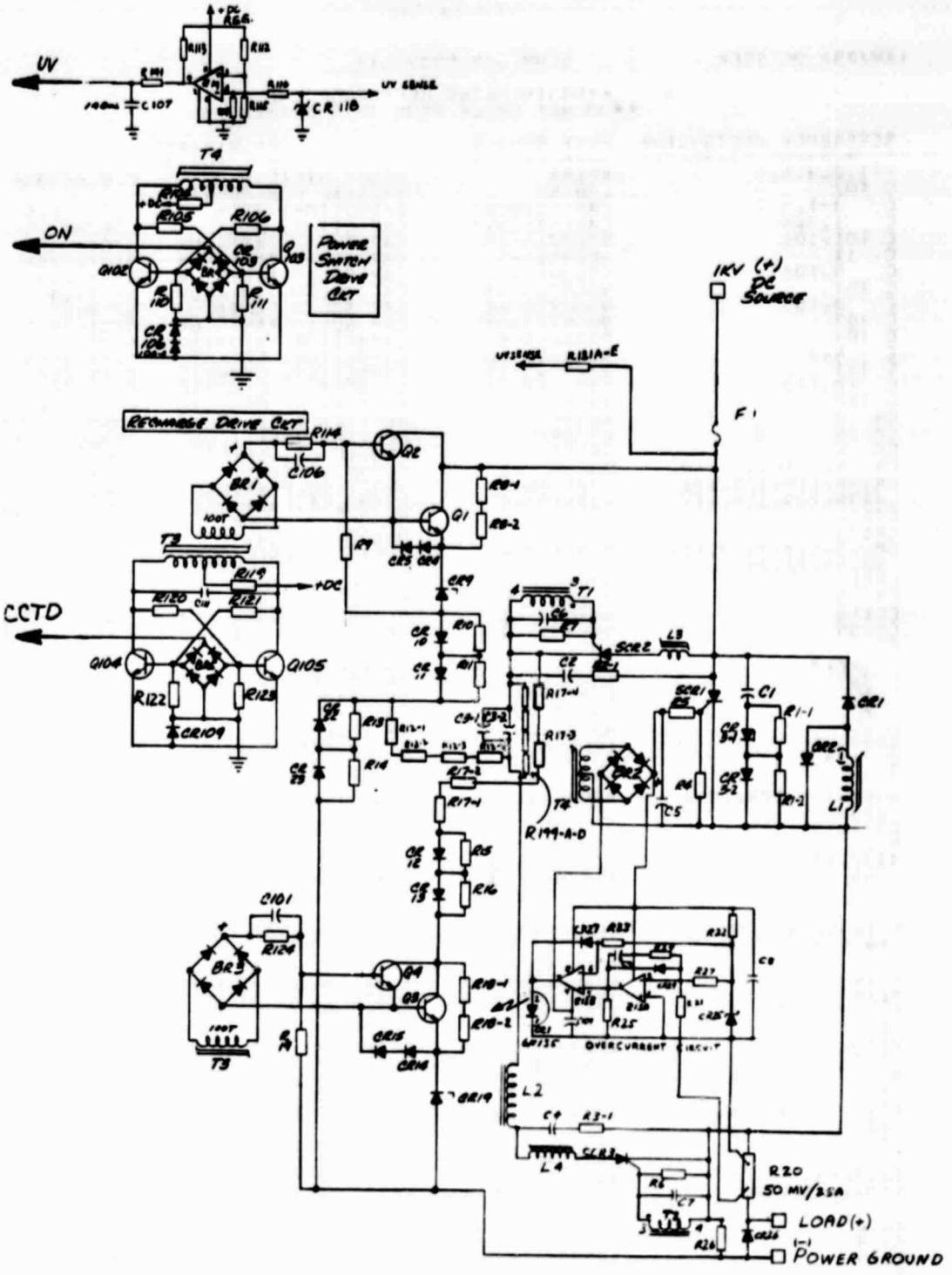


Figure 5-3

1 KV/25A DC SSPC Schematic Diagram (Continued)

Table 5-1

Parts List

1KV/25A DC SSCB SCHM DGM E0393617

ENGINEERING REFERENCE ONLY
DO NOT ORDER FROM THIS DRAWING

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	
BR1,2,3,4,5	VE18X	DIODE,SILICON	F.W.BRIDGE ASSY
C 102	.001MF	SPECIAL COMPONENT	
C 3-1,3-2	CMR1A3299SP	CAPACITOR, MICA	3.75MF/2500V
C 1,2,4	CMR1A3309SP	CAPACITOR, MICA	.068MF/2500V
C 101,106	9060715-19	CAP SOLID TANTALUM	3/01-2306 .22U 35VK
C 11	9060715-2	CAP SOLID TANTALUM	3/01-2283 2.2U 20VK
C 5,108	9060715-22	CAP SOLID TANTALUM	3/01-2338 0.1U 35V5
C 107	9060715-43	CAP SOLID TANTALUM	SP T110 1.0U 35VK
C 8,105	9060715-46	CAP SOLID TANTALUM	SP T110 3.9U 35VK
C 103	9060715-62	CAP SOLID TANTALUM	3/01-2326 .022U 35VK
C 104	930A654-16	CAPACITOR, ALUMINUM	6000 100U 75VF
C 6,7	932A745-1	CAPACITOR, CERAMIC	14/1-1593 .1U 50VK
C 111	932A745-11	CAPACITOR, CERAMIC	14/1-1575 .01U100VK
C 10,110	932A745-19	CAPACITOR, CERAMIC	3300P/100V
C 112	932A745-21	CAPACITOR, CERAMIC	82P/200V
CR 2	A139P	RECTIFIER,SILICON	1000V 30A GE
CR 26	A170RPE	RECTIFIER,SILICON	1500V/100A REV POLAR
CR 1	A177PE	RECTIFIER,SILICON	1500V 100A FSW GE
CR 4,5,14,15,110	9060976-1	DIODE,SILICON	J645 225V .4A DO7
CR106,119,120,121	927A496-2	DIODE,SI,FAST,REC	J4148 75V .1A DO35
CR106,109,116,117	927A496-6	DIODE,SI,FAST,REC	914 75V .1A DO7
CR101	929A430-4	DIODE,SI,ZENER	4734A 5.6V5P1WDO41
CR104	929A434-1	DIODE,SILICON	J486B 225V.2A DO7
CR 3-1,3-2,10,11, 12,13,22,23	929A678-6	RECTIFIER,SILICON	4007 1000V 1A A16V
CR111	929A680-1	DIODE,SI,ZENER	UZ713 13V5P3W A60
CR 9,19	931A684-5	DIODE,SI,ZENER	5343B6.8V5P5W A1EE
CR118	938D392-16	DIODE,SI,ZENER	47V 5P-.05M.4W DO7
CR105	938D392-9	DIODE,SI,ZENER	12V 5P-.05M.4W DO7
F1	NOS-35	FUSE	35A
I 1,2,3	956C772-2	INDICATOR	LAMP,NO,327
L 3,4	ED387575	INDUCTOR	5MICROH
L 1	ED387576	INDUCTOR	50MICROH
L 2	ED387577	INDUCTOR	380MICROH
OC1	932A762-4	OPTICAL COUPLER	6N135 TR.05 DR
Q107	IRF306	FIELD EFFECT TRAN	MOSFET 350V/5A
Q 1,2,3,4	MJ12005	TRANSISTOR, NPN,PWR	12A/1500V MOTOROLA
Q101	929A433-3	TRANSISTOR,PNP	J2904A 60V.6A TO5
Q102,103,104,105, 106	929A433-6	TRANSISTOR, NPN	J3019 80V 1A TO5
Q108,109,110	929A676-4	TRANSISTOR, NPN	2222A 40V .8A TO18
R 20	*SHUNT-25A	SPECIAL COMPONENT	50MV/25A
R132,134	RC07GF150J	RESISTOR CARB COMP.	15-OHMS .25W TOL 5
R133	RC07GF912J	RESISTOR CARB COMP.	9.1K T5 .250W RC07
R131,131,131,131, 131	RC42GF225J	RESISTOR CARB COMP.	2.2M T5 2.0W RC42
R 26-1,26-2,26-3, 26-4,26-5	RC42GF393J	RESISTOR CARB COMP.	1 39K T5 2.0W RC42
R130	RN60D4023F	RESISTOR METAL FILM	402K T1 .125W RN60D
R 24	RN60D4753F	RESISTOR METAL FILM	475K T1 .125W RN60D
R129	RN60D8063F	RESISTOR METAL FILM	806K T1 .125W RN60D
R 1-1,1-2	11D3300-14	RESISTOR CARB COMP.	47 T10 1.0W RC32
R125	11D3300-58	RESISTOR CARB COMP.	10 T10 1.0W RC32
R120,121	18D3546-11	RESISTOR CARB COMP.	24K T5 .250W RC07
R142	18D3546-12	RESISTOR CARB COMP.	1K T5 .250W RC07
R 5	18D3546-19	RESISTOR CARB COMP.	10 T5 .250W RC07
R104	18D3546-21	RESISTOR CARB COMP.	100 T5 .250W RC07
R110,111,122,123, 127	18D3546-26	RESISTOR CARB COMP.	4.7K T5 .250W RC07
R141,143	18D3546-29	RESISTOR CARB COMP.	150K T5 .250W RC07
R126	18D3546-33	RESISTOR CARB COMP.	51 T5 .250W RC07
R107,135	18D3546-34	RESISTOR CARB COMP.	100K T5 .250W RC07
R108,113,128	18D3546-39	RESISTOR CARB COMP.	10K T10 .250W RC07
R105,106,145	18D3546-48	RESISTOR CARB COMP.	47K T10 .250W RC07
R118	18D3546-5	RESISTOR CARB COMP.	470K T5 .250W RC07
R137	18D3546-50	RESISTOR CARB COMP.	1M T10 .250W RC07
R119	18D3546-52	RESISTOR CARB COMP.	27 T5 .250W RC07
R136	18D3546-59	RESISTOR CARB COMP.	51K T5 .250W RC07
R109	18D3546-85	RESISTOR CARB COMP.	5.6K T5 .25W RC07
R 2-1,3-1	908D276-20	RESISTOR CARB COMP.	10 T5 2.0W RC42
R 12-1,12-2,12-3, 12-4,17-1,17-2, 17-3,17-4	908D276-22	RESISTOR CARB COMP.	110 T5 2.0W RC42
R114,124	909C790-41	RESISTOR CARB COMP.	510 T5 0.5W RC20
R 4,6,7	909C790-46	RESISTOR CARB COMP.	51 T5 0.5W RC20

Table 5-1

Parts List (Continued)

1RV/25A DC SSCB SCHM DGM ED393617

ENGINEERING REFERENCE ONLY
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REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	
R 9,19	909C790-55	RESISTOR CARB COMP.	1K T5 0.5W RC20
R 8-1,8-2,10,11,13, 14,15,16,18-1,18-2	909C790-92	RESISTOR CARB COMP.	6.8M T5 0.5W RC20
R103	928A736-15	RESISTOR METAL FILM	499 T1 .125W RN60D
R102	928A736-21	RESISTOR METAL FILM	1.00K T1 .125W RN60D
R101	928A736-49	RESISTOR METAL FILM	82.5K T1 .125W RN60D
R116,117	928A736-53	RESISTOR METAL FILM	150K T1 .125W RN60D
R112,115	928A736-57	RESISTOR METAL FILM	301K T1 .125W RN60D
R144,144,144,144	928A739-35	RESISTOR CARB COMP.	10M T10 0.5W RC20
R138,139,140	932A720-10	RES.F.COMP .250W T5	RCR07G512JS 5.1 K
R146	932A724-22	RES.F.FILM .125W T1	RNC60H4993FS 499. K
SCR 1,2,3	T50T1540S5AA	THYR.SCR.INV TYPE	1500V 100A WEST
T 3	ED387578	TRANSFORMER, PULSE	ROYER 600T-T-600T RC
T 4	ED387579	TRANSFORMER, PULSE	ROYER 600TCT-60T PSW
T 1,2	306-0218	TRANSFORMER, PULSE	1-1 RATIO KLADDIN
Z01	LM10H	LIN COMPARATOR	10[illegible] COR
Z03,08	MC14001BAL	CMOS	QUAD2INNOR14001BAD14
Z07	MC14025BAL		CMOS TRIP[illegible] 3IN NOR
Z14	933A200-1	LIN COMPARATOR	ONS LIL DI4
Z02,09,12	933A882-1	CMOS	HEX INV 4049UBD16
Z06,11	933A905-1	CMOS	DUAL D FF 4013BAD14
Z05	933A907-8	CMOS	4 [illegible]ORGATE 4070BAD14
Z04,10	933A911-1	CMOS	2-BIT UP CO14520BAD16

* Both transformers use #36 wire for primaries, #26 wire for secondaries and Magnetics, Inc. #80525-1A cores.

5.3.1 Control Functions

5.3.1.1 Control Power and Regulated Power Supply

Control power is provided by an external 28 VDC supply with a nominal current of .1 ADC. In addition to feeding the regulated supply, the +28 VDC is also directly connected to voltage divider R101 and R102 of the low voltage comparator and the high side of the indicator lamps. In the regulated supply, unregulated DC appears at the collector of Q106, feeding the control switch interface, the power switch drive, recharge drive, and commutation drive circuits. 12 VDC appears at the emitter, the reference established by CR111, a Zener diode. This regulated supply feeds all the logic circuits and is necessary for uniformity of reference, especially in the fault protection circuitry.

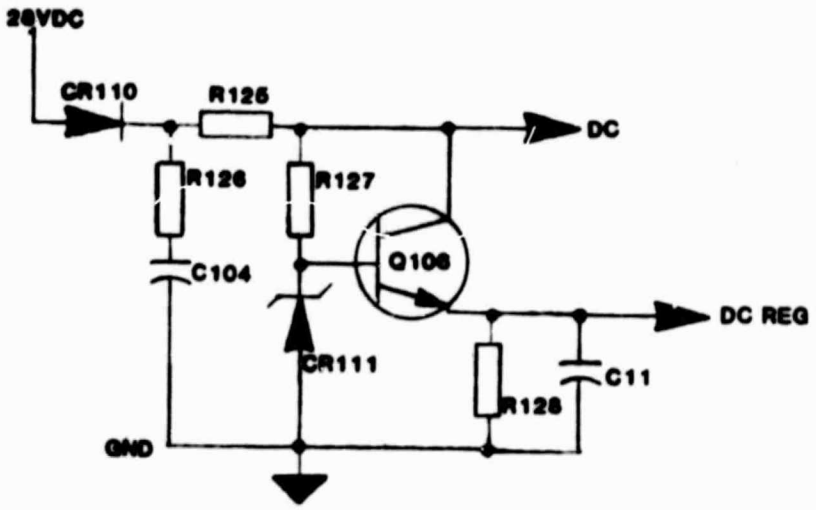


Figure 5-4

Power Supply

5.3.1.2 Control Switch and Time Delay

The purpose of the control switch is to provide an external interface to a remote control point. The time delay provides operating stability. Z3B, Z3C, Z5A, and Z6A operate as a toggle producing a Logic 1 for ON and Logic 0 for OFF at Z6, Pin 2. Z5B and Z4B provide 8 milliseconds by a change of state of Z4, Pin 14. This signal, through inverter Z2D, is routed to the power drive switch ON section at Z7A.

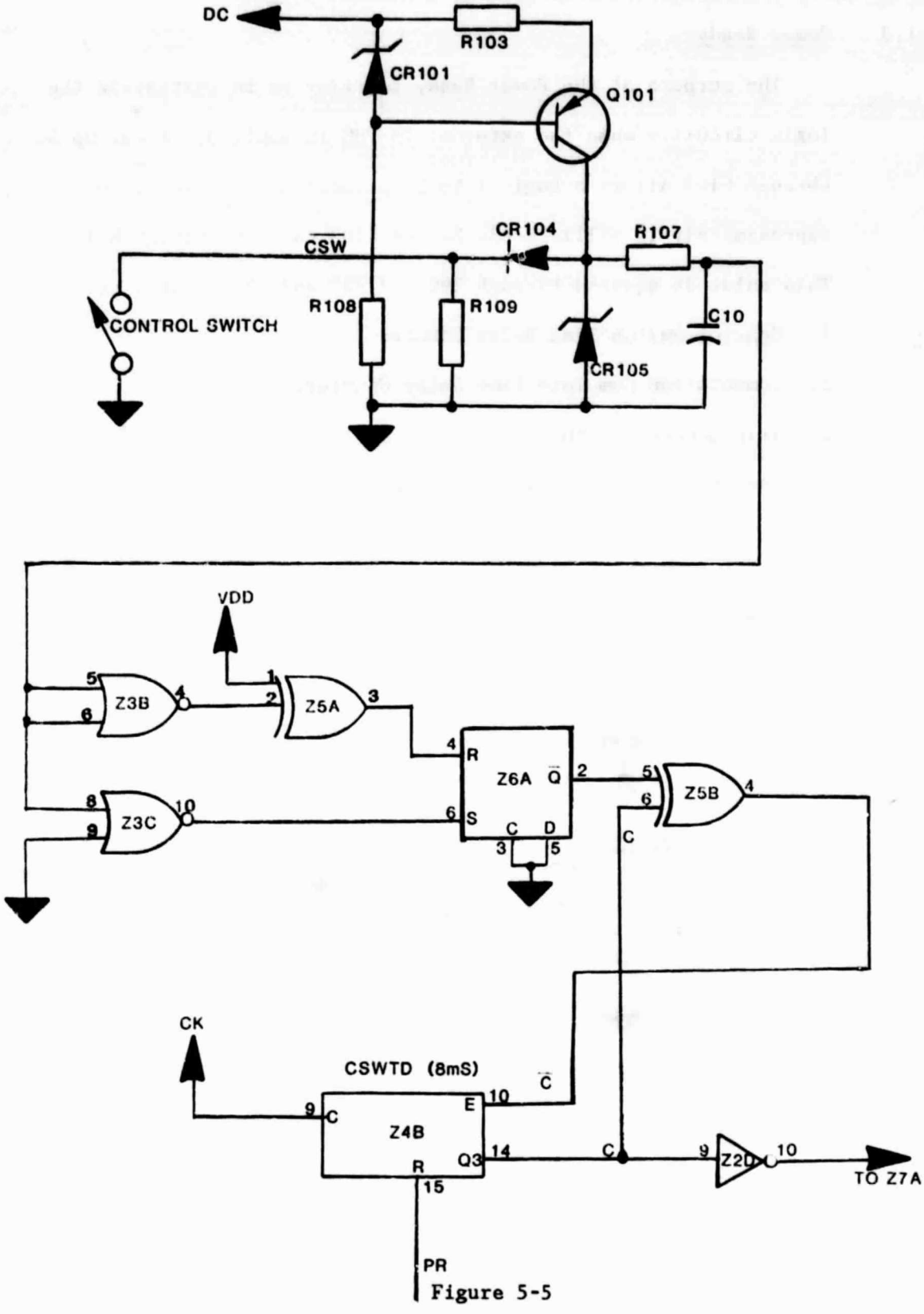


Figure 5-5

Control Switch and Time Delay

5.3.1.3 Power Ready

The purpose of the Power Ready function is to initialize the logic circuitry when the external 28 VDC is applied. Power up DC through C103 allows a Logic 1 to be present at Z9, Pin 7, for approximately 10 milliseconds before C103 charges through R118. This pulse is squared through Z9C and Z9D and then routed to:

1. Control Switch Time Delay Counter,
2. Commutation Complete Time Delay Counter,
3. Trip Lockout Latch,
4. Commutation Driver Time Delay Counter, and
5. Recharge Drive Circuit.

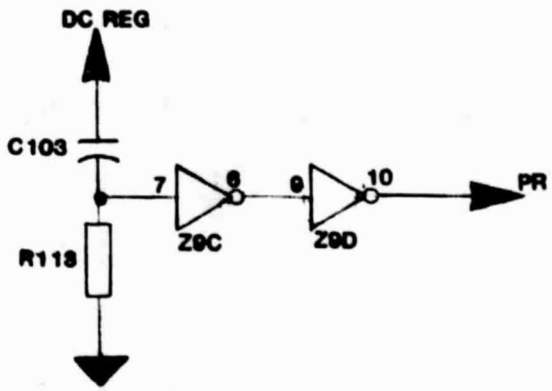


Figure 5-6

Power Ready

5.3.1.4 Trip Lockout

The purpose of the TLO is to lock the SSPC in the OFF position in the event of power undervoltage, power overcurrent, or control undervoltage, preventing ON/OFF cycling. Z6B is configured in a set/reset mode. Initially, Pin 13 is low, having been reset by the PR signal. A trip signal from OC, UV, or LVTD through Z8A and Z9A sets the latch and Pin 13 goes high, turning the power switch drive off through Z7A. This condition remains (even if the set signal is removed) until the latch is reset either by PR (remove and reapply 28 VDC) or cycling the control switch. C112 and R146 provide noise immunity and loading for the OC and UV circuits being combined at Z8A, Pin 2, through CR119 and CR120.

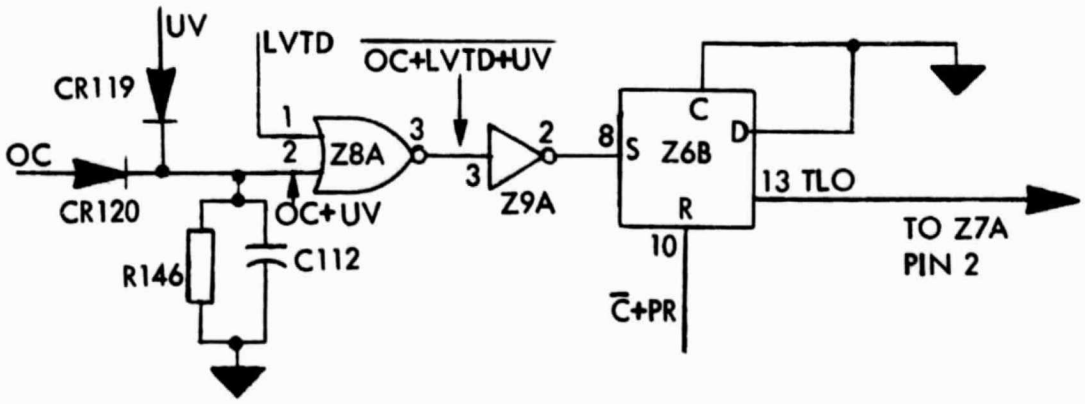


Figure 5-7

Trip Lockout

5.3.1.5 Power Switch Drive Circuit

The purpose of the power switch drive circuit is to turn on the power controller (SCR1) and provide logic to power isolation. A Royer oscillator is employed to provide the isolation for the ON/OFF action. BR2 at the secondary of T4 provides DC gate voltage to turn on SCR1. BR2 also provides power to the OC circuit.

5.3.1.6 Power Switch

The power switch consists of a single SCR (SCR1) which is turned on by gate voltage from the power switch drive circuit. The SCR is turned off by removing the gate drive and forcing the current through the SCR to zero by means of the commutation circuit.

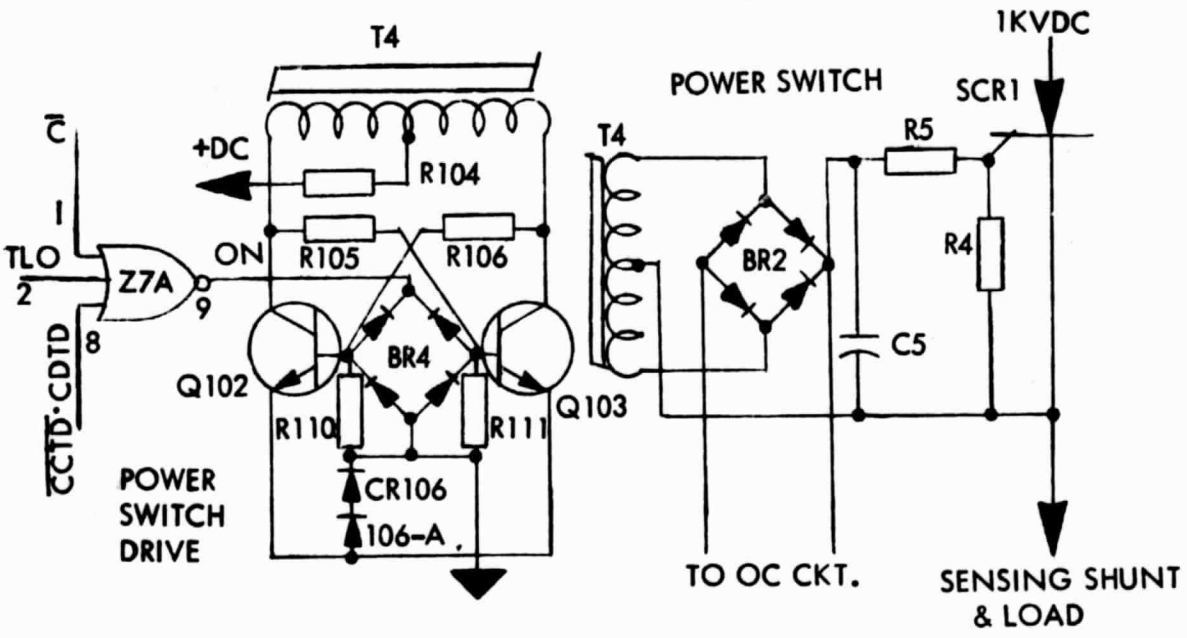


Figure 5-8

Power Switch and Power Switch Drive Circuits

5.3.1.7 Commutation Drive Circuit

The purpose of the commutation drive circuit is to initiate the commutation while providing isolation between logic and power circuits. When the commutation signal at Z11, Pin 13, goes high, MOSFET Transistor Q107 fires drawing a current pulse from C105 through pulse transformers T1 and T2. The secondaries of these tranformers provide firing pulses for SCR2 and SCR3 circulating commutation current from energy stored in C3-1 and C3-2.

L1 and CR1 provide a path for excess current after SCR1 is shut off, and produce a reverse voltage to insure shut-off.

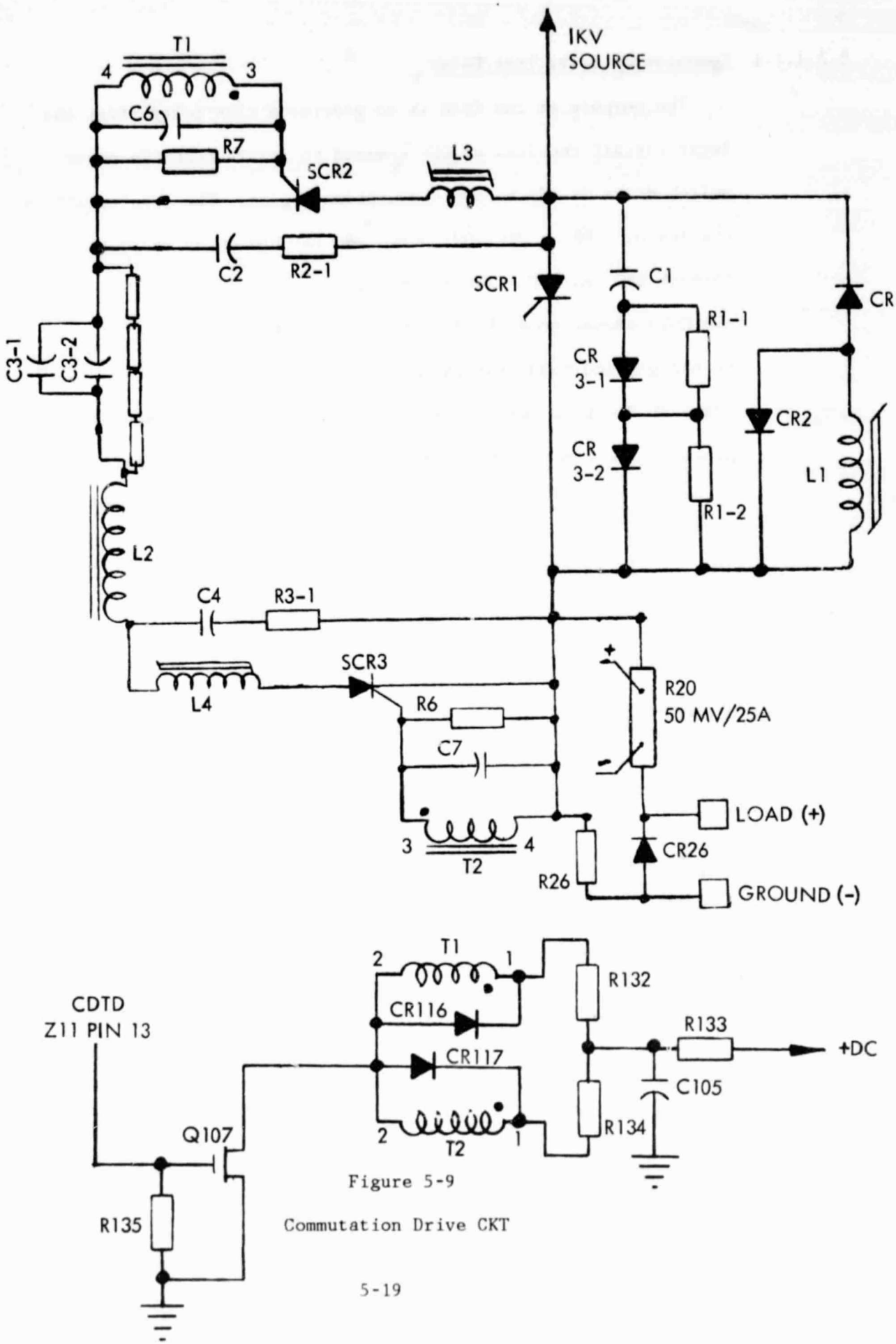


Figure 5-9

Commutation Drive CKT

5.3.1.7.1 Commutation Drive Time Delay

The purpose of the CDTD is to provide a time delay after the logic circuit receives an OFF command to insure that the power switch drive is off before commutation begins. The counter Z11 is started by a PR or OFF ($\overline{ON}$) pulse and latched on by its output through Z8C and Z9F. After commutation, the counter is reset by the CCTD signal from Z5, Pin 10, to cut off Q107 so that C105 will be charged and ready for the next commutation. Commutation takes place at Power Up and any OFF or TRIP. Commutation also takes place at the removal of control voltage, the action being powered by residual charge in C104 and C11 and initiated by the LVTD TLO.

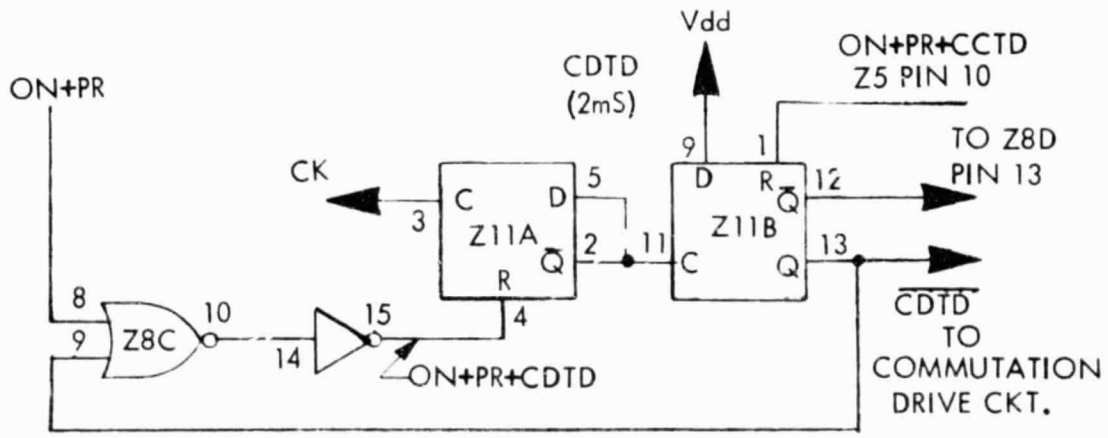


Figure 5-10

Commutation Drive Time Delay

5.3.1.8 Recharge Drive Circuit

The purpose of the recharge drive circuit is to provide logic-to-power circuit voltage isolation and to maintain a charge on the commutation capacitors. This is accomplished by using a Royer oscillator to transformer couple the logic circuit to the power circuit. When Z5, Pin 10, goes high (recharge on), the bases of Q104 and Q105 are released from ground clamp and the circuit begins to oscillate. BR1 and BR3 powered by the secondaries of T3 provide drive to Q1, Q2, Q3, and Q4, providing a current path to charge C3-1 and C3-2. During commutation, the oscillator is clamped off and Q1, Q2, Q3, and Q4 are cut off, preventing a direct current path from the source to ground or the load through the commutation SCR's.

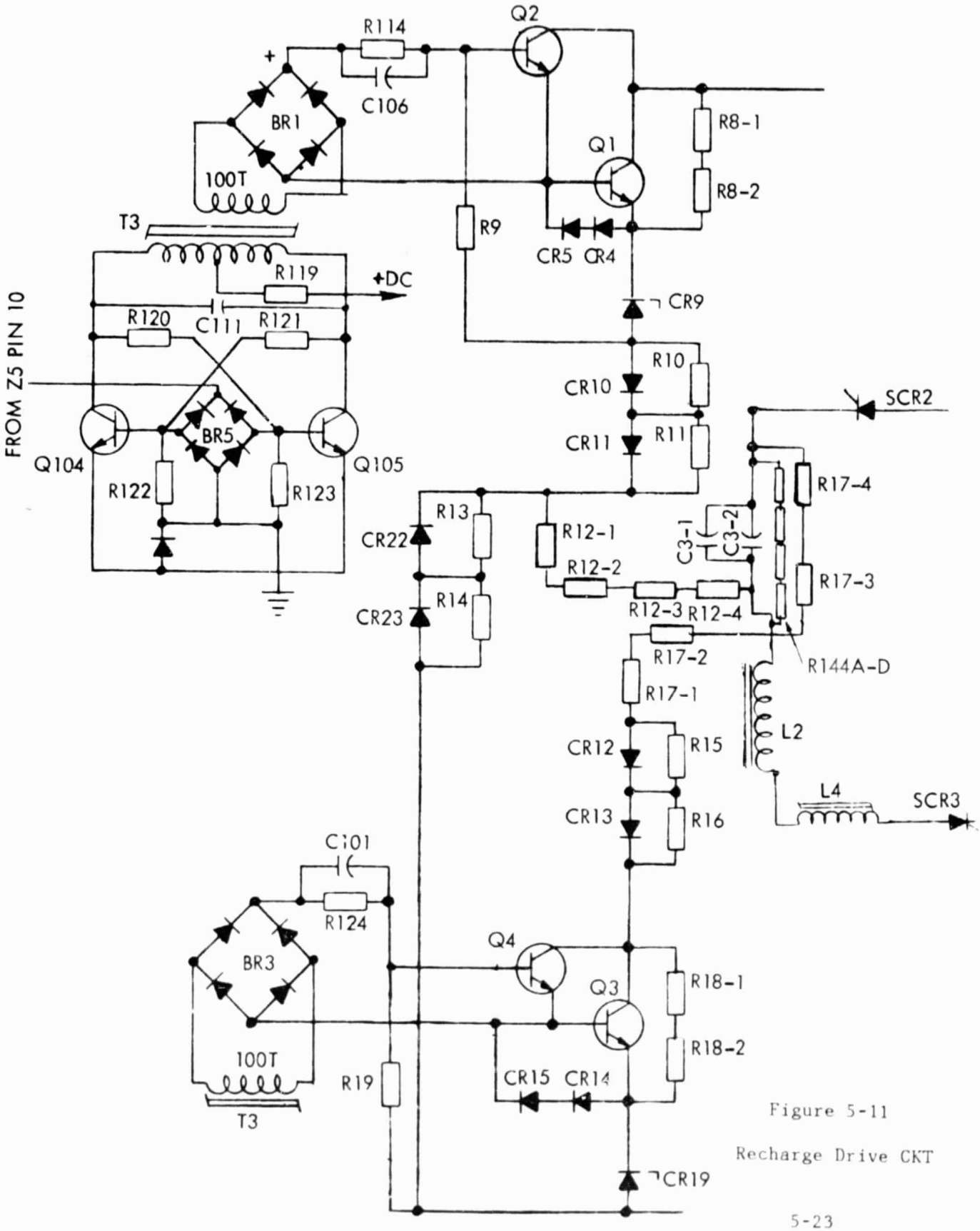


Figure 5-11

Recharge Drive CKT

5.3.1.8.1 Commutation Complete Time Delay

The purpose of the CCTD is to shut off the recharge drive circuit during commutation so that the commutation current is routed properly to shut off the power to the load (shut off SCR1). The time delay counter is initialized by the trailing edge of the PR or $\overline{ON}$ signals at the Reset Pins 7 and 15 of Z10. When the TD (128 milliseconds) is complete, the output is latched high at Pin 14. Coupled through Z7C and Z5C, the CCTD provides a 128 millisecond hole in the recharge drive circuit operation. The CCTD coupled with the commutation drive TD and inverted ($\overline{CCTD}$ • CDTD) is routed to the ON logic at Z7A through a 10 millisecond time delay to allow the recharge circuit to operate for 10 milliseconds before the power switch drive comes on to obtain a full charge to commutate if the switch comes up into an OC fault.

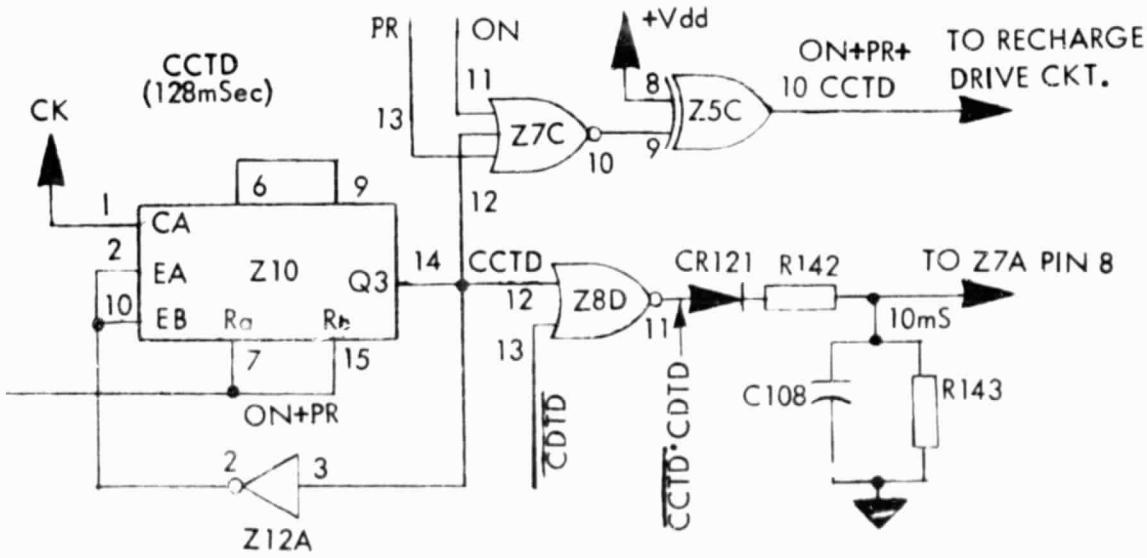


Figure 5-12

Commutation Complete Time Delay

5.3.1.9 Clock

The purpose of the clock is to provide a time base for the various time delay counters. Inverters Z12B and Z12C form an oscillator whose frequency is determined by R129, R130, and C102. The approximately 1 KHz clock signal is buffered by Z12D and distributed to the clock inputs of the counters.

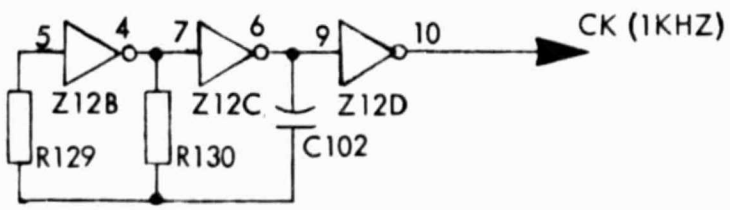


Figure 5-13

Clock

5.3.2 Protection Functions

5.3.2.1 Overcurrent

The purpose of the overcurrent circuit is to monitor load current and provide a trip signal when the current level exceeds the minimum threshold. The trip time is shorter the greater the overcurrent. Load current is sensed in Calibrated Shunt R20 and the proportional voltage (2mV/amp) applied to Z13A through R21. R22 and CR25 provide a stable reference. When the current (thus the shunt voltage) exceeds the reference, Z13A integrates, increasing the voltage at Pin 1 at a rate proportional to the excess When the voltage at Pin 1 exceeds the reference (Z13B, Pin 6), Pin 7 goes positive firing Optocoupler, OC1, sending the trip signal to the logic circuit. OC1 provides isolation between the high voltage bus and the logic circuit. R145 and C110 prevent false trips caused by transients in the commutation path of 100 μseconds or less duration. The OC circuit is energized by the power switch drive circuit, thus only operational in the ON state. Tripping is almost instantaneous, however, under heavy load conditions. Diodes CR27 and CR24 enhance speed of operation by affecting non-saturated mode of operation for Z13A and Z13B.

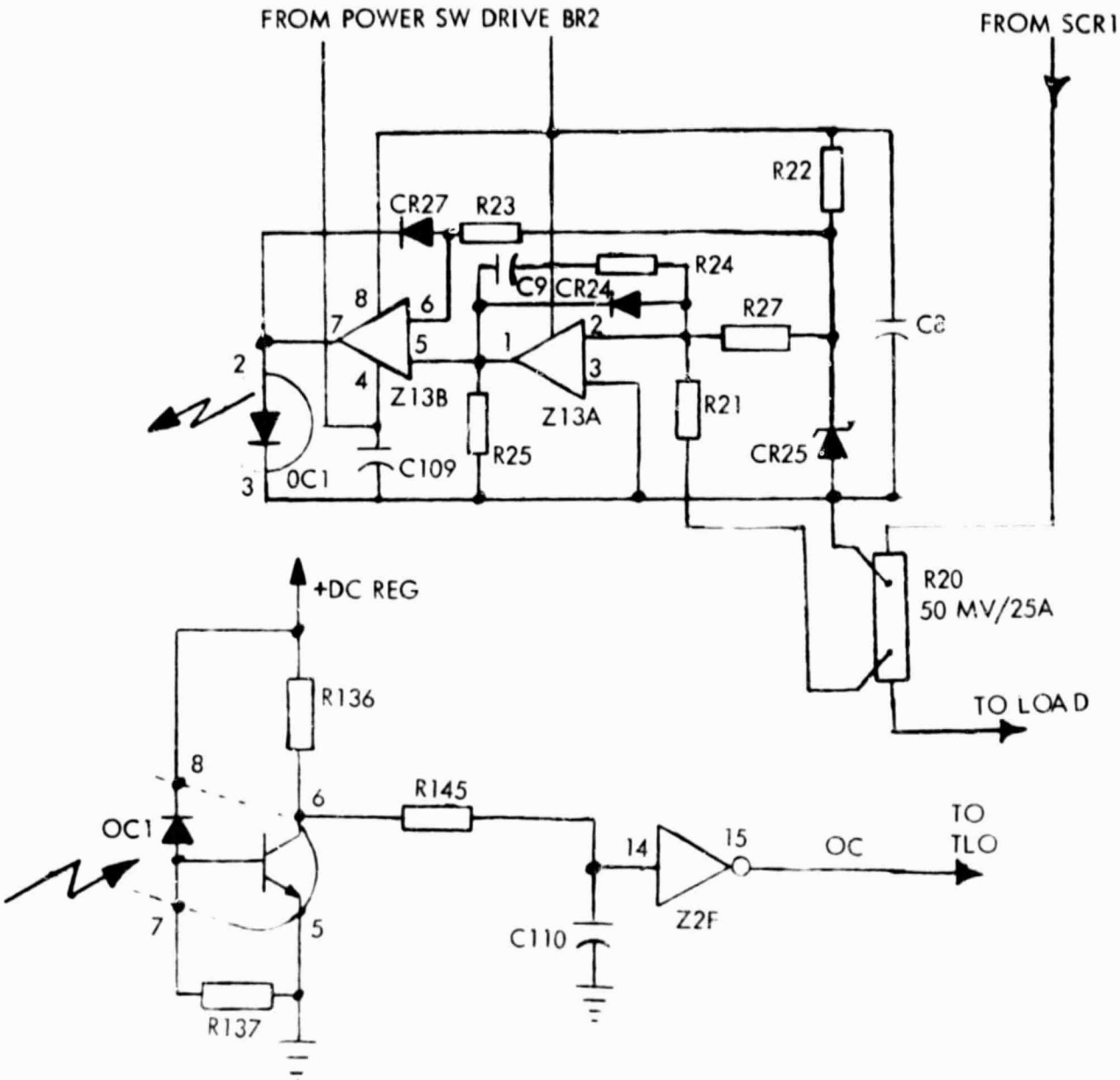


Figure 5-14

Overcurrent Circuit

5.3.2.2 Low Voltage

The purpose of the low voltage circuit is to shut off the power controller when the control voltage drops below a level necessary for proper operation. The reference level set by R101 and R102 provides a Logic 1 at Pin 6 of Z1A for normal voltage or $\overline{LV}$, Logic 0, for LV. A low voltage condition releases the LV time delay counter and allows it to count under either of two conditions: (1) LV with power controller on, (2) attempted turn-on (control switch) with LV condition. The 8 millisecond time delay prevents transient voltage fluctuations from tripping the circuit as any LV of less duration will reset the counter before a LVTD output appears at Z4, Pin 6. The LVTD is coupled to the TLO through Z8A.

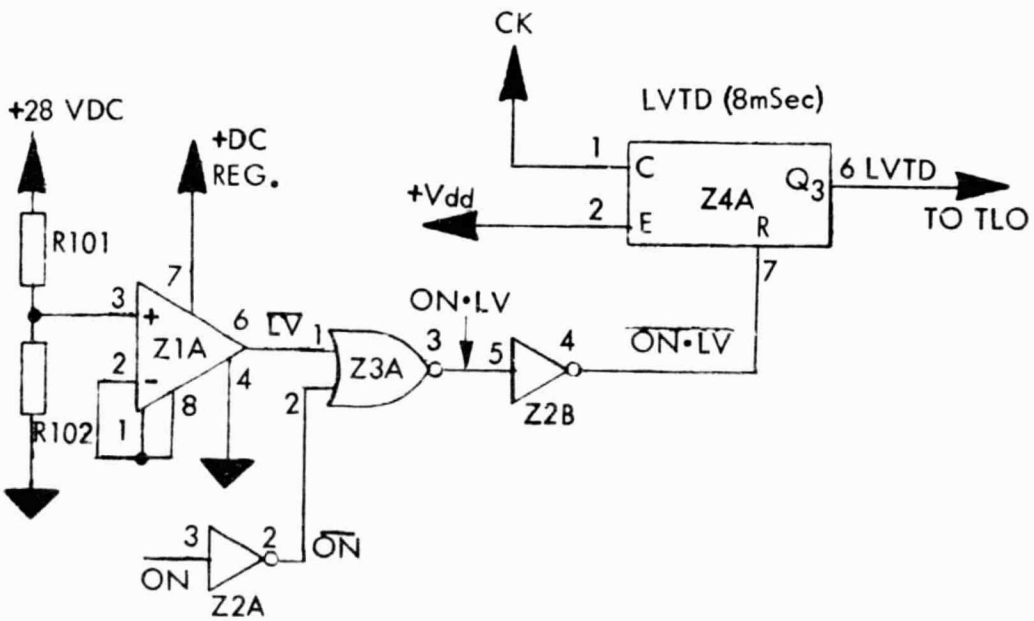


Figure 5-15

Control Low Voltage Time Delay

5.2.2.3 Undervoltage

The purpose of the undervoltage circuit is to shut off the power controller when the DC source voltage drops below approximately 450 volts. R131, R116, and R117 provide 6V at Z14, Pin 4, at this level. R112 and R115 provide a 6V reference at Pin 3. When the DC source voltage drops below 450 volts, Pin 4 goes below the 6V reference, producing an output at Pin 9. The UV signal then passes through a 140 millisecond time delay, R146, R141, and C107, and is coupled to the TLO circuit through CR119. As in the LV circuit, the time delay prevents nuisance trips.

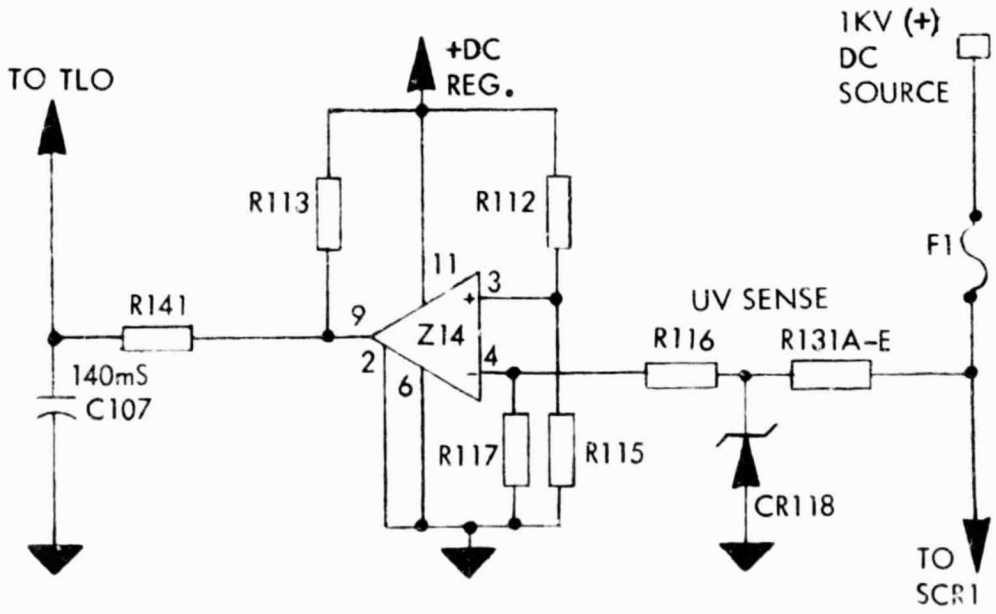


Figure 5-16

Undervoltage

5.3.3 Indicator Circuits

The purpose of the indicator circuit is to provide visual indication of the status of the power controller. Logic signals for ON, OFF, and TRIP appear at Z7, Pin 9, Z2, Pin 12, and Z6, Pin 13, providing drive to Q109, Q108, and Q110, through R139, R138, and R140 respectively, energizing the 28V lamps for each function.

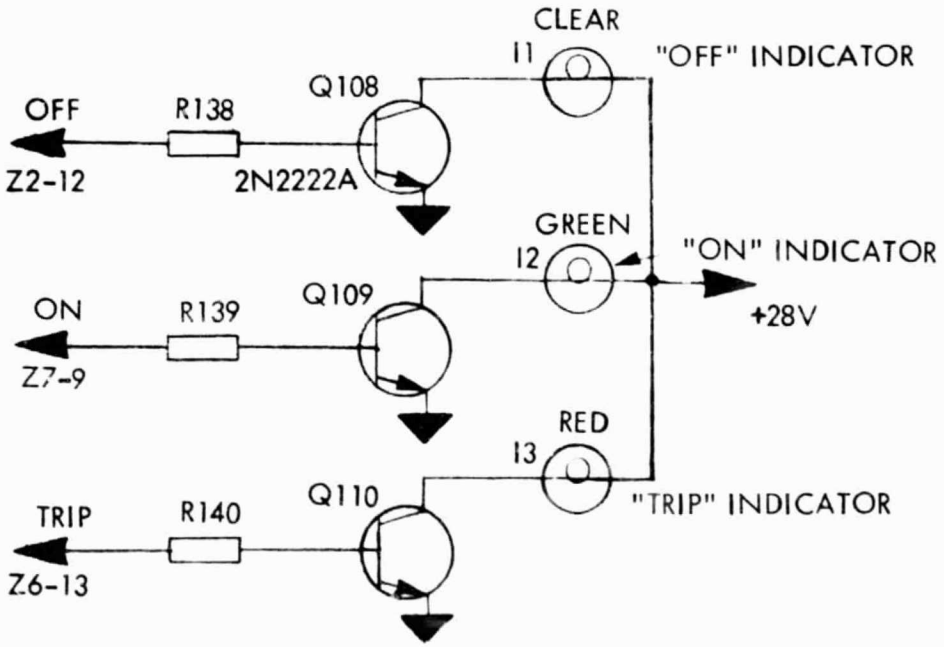


Figure 5-17

Indicator Circuit

5.4 1 KV/25A SSPC Test Data

A summary of test data is shown in Table 5-2 and Figures 5-18 through 5-20. All data was taken at room ambient.

Table 5-2

Significant Test Data

Control Power @ 28 VDC	2.4-2.6	Watts
Undervoltage Protection:		
Operation	428-465	VDC
Time Delay	66	msec.
Low Voltage Protection:		
Operation	16.7	VDC
Time Delay	8	msec.
Overcurrent Protection	See Figure 5-19	
Turn-On/Turn-Off Time Delay	8	msec.
Power Switch Voltage Drop, 0-25 ADC	1.3	VDC
Total Power Dissipation @ 25 ADC	34.4	Watts
Efficiency at 25A/1000 VDC	99.86	%

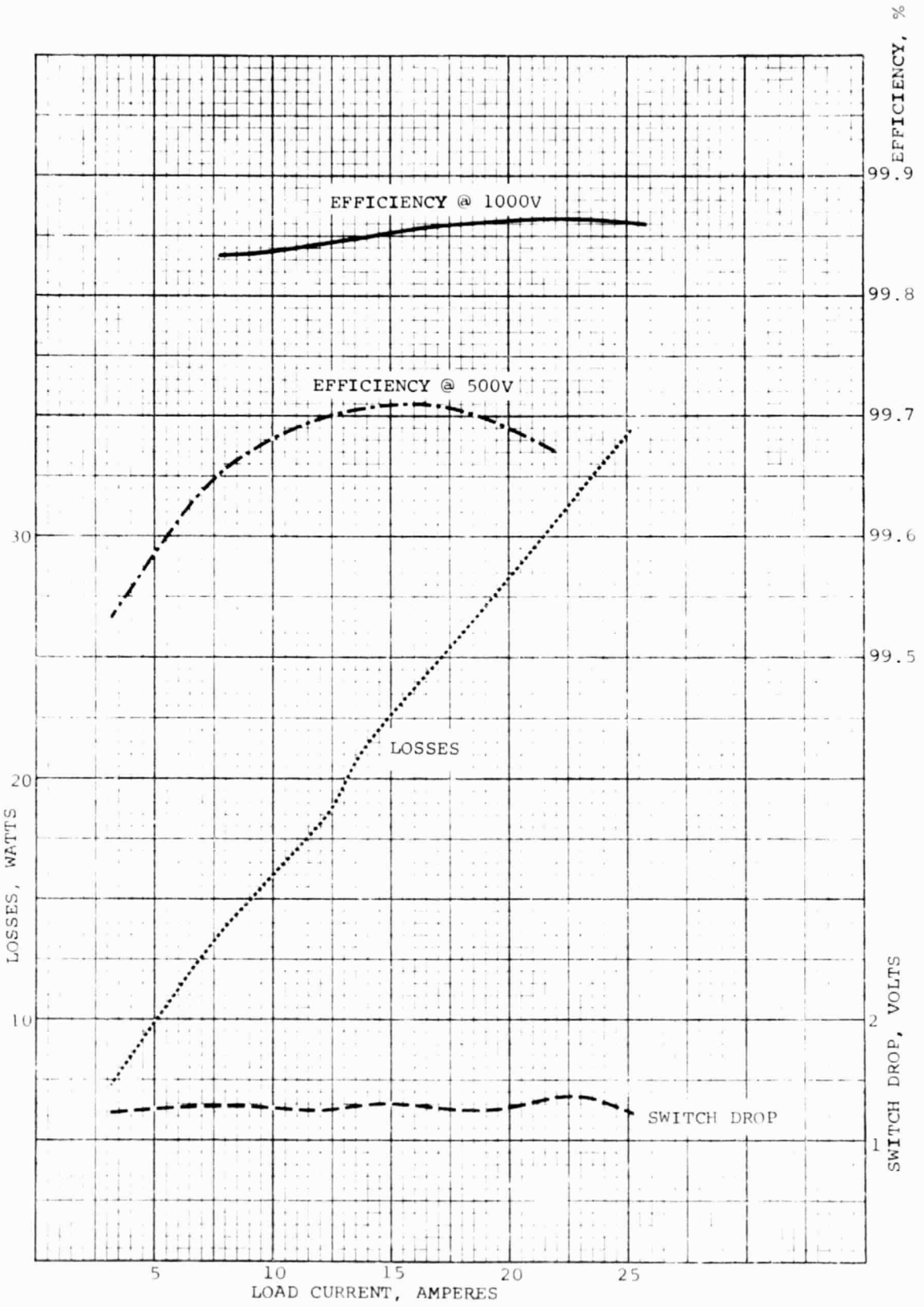


Figure 5-18

Efficiency, Losses, and Switch Drop Vs. Load Current

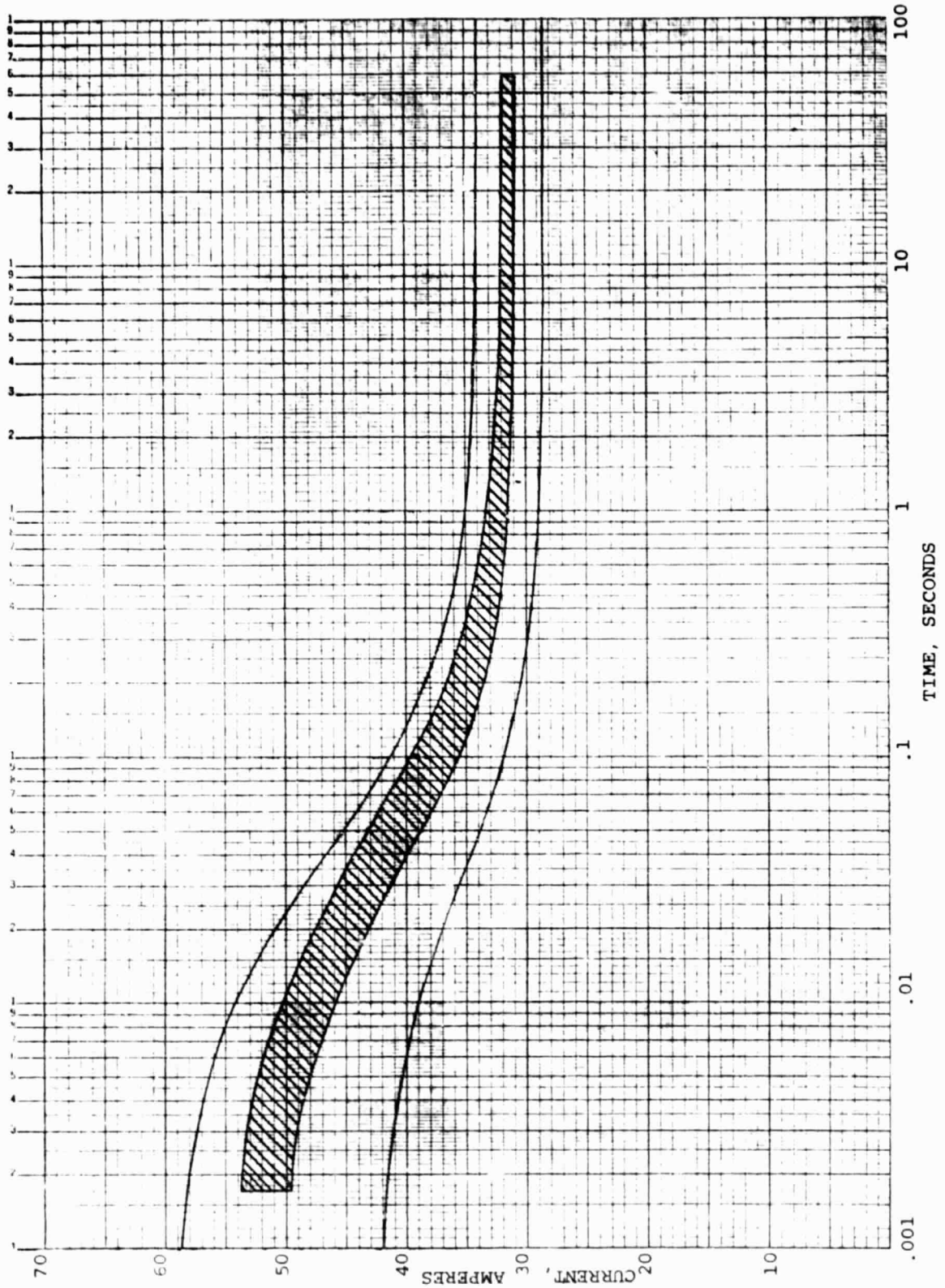
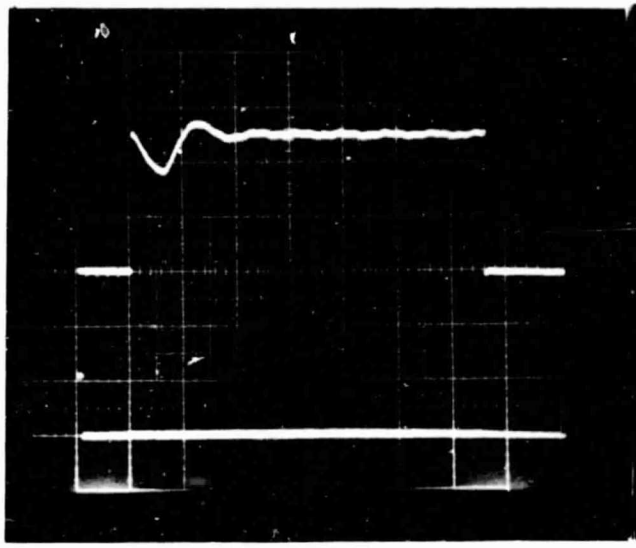


Figure 5-19

Performance Data Loci - 1 KV/25A DC SSPC Breadboards

Turn-Off and Trip-Off (50A/1 KVDC)

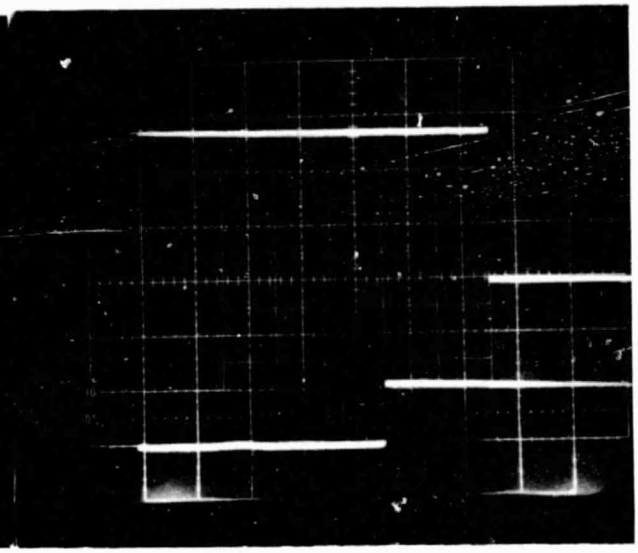


Top: Load Current, 20A/div.

Bottom: Control Switch Volt, 10V/div.

Time: 10 msec./div.

Turn-Off (25A/500 VDC)

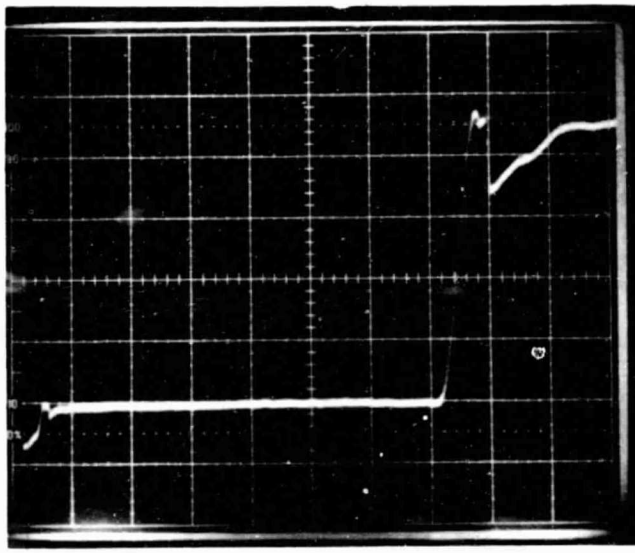


Top: Load Voltage, 200V/div.

Bottom: Control Switch Volt, 10V/div.

Time: 5 msec./div.

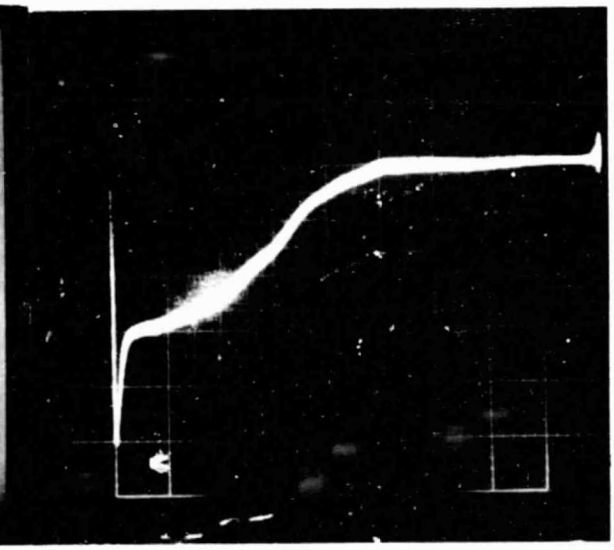
Power Switch Turn-Off (25A/1 KVDC)



V (SCR1): 200V/div.

Time: 20 μsec./div.

Power Switch Revised Bias (50A/500V)



V (SCR1): 20V/div.

Time: 10 μsec./div.

Figure 5-20 - 1 KV/25A SSPC Oscilloscope Pictures

5.5 Amended Task Objectives

In September, 1979, the program was amended to extend the operating voltage range lower limit from 500 VDC to 200 VDC and perform trade-off studies to establish operating parameters and characteristics for switchgear and this extended operating voltage range by analyzing and comparing concepts and designs for the following two options:

I. Option 1

One switchgear type that will meet all specifications while operating over the voltage range from 200-1100 VDC.

II. Option 2

Two types of switchgear that span the operating voltage range in two steps.

Type A: Meets all specifications as listed.

Type B: Has the following specifications:

Rated Voltage:	300 ± 100 VDC
Operating Voltage Range:	200 to 500 VDC
Rated Current:	80A (100A Max.)
Max. Voltage Drop:	0.2V @ 80A
Max. Power Dissipation:	ON Equal to 20W, OFF Equal to 0.2W

5.6 Prologue to Design Analysis

In the previous program efforts of Tasks I and II, 25A/1 KVDC SCR type solid state switch breadboards were designed, fabricated, and successfully evaluated over operating voltages of 200-1000 VDC* and load currents of 2.0 to 50 amperes. In considering Option I, this design would suffice for the listed requirements, except for overload clearance capability at 200 VDC. An additional consideration is the increase in size and weight to meet the required overload capability at 200 VDC due to a significant enlargement in commutation current elements. Therefore, the following analysis focuses on Option II (B) with the present 1 KV/25A design for filling the Option II (A) requirements.

*1100 VDC testing was precluded by power supply voltage limitation.

5.7 Design Analysis

5.7.1 Comparison of Electro-Mechanical and Solid State HVDC Power Switches

Originally, the Westinghouse internal HVDC switching development program was directed toward a 270 VDC/150A/40 KW aircraft system. This system was powered from a conventional generator with fault current limiting 250% of rated current. As a result, the electro-mechanical device and SCR-type shut-off circuitry was rated for 400-500 ampere interrupt capacity. This overload rating exclusively determined the size of the power relay. This occurs because the output current will achieve its steady state fault current level before the electro-mechanical device can transfer to the open position.

Consequently, the power switch must be designed with the source impedance (fault current) as the primary concern, because if the source is not limited (zero impedance), the electro-mechanical switch is an impractical device for the application. To expand on this, if the breaker trip time is 20 milliseconds maximum and the maximum fault current is to be limited to 350 amperes (assuming the trip level was sensed at 100 amperes), a 500 volt, 40 millihenry series choke is required to be inserted into the system (see Figure 5-21).

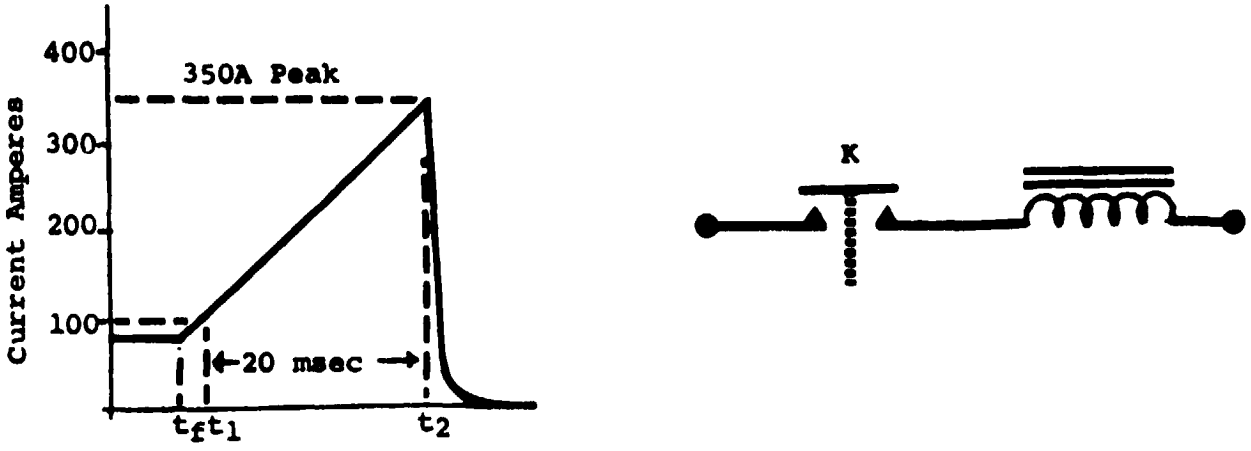


Figure 5-21

To meet actual switch drop of .2V, this inductor would have to be designed to offer no more than .05-.1 volts drop at rated current which places a severe restraint on the winding size. The estimated size and weight for this inductor is 48" x 40" x 37" or 1.2 x 1.0 x .94m, and 12,000 pounds or 5400 kilograms.

Another approach would be to use a power transistor as the main switching element. If the transistor storage and fall times are assumed to be 4×10^{-6} seconds maximum and the allowable peak current is to be 140 amperes*, the series limiter choke, L, can be reduced to 50 μH as illustrated in Figure 5-22.

*The maximum allowable peak current is determined primarily by the capability and design of the power switch and drive circuits; 140A is based upon 175% rated capability to assure providing the 150% required.

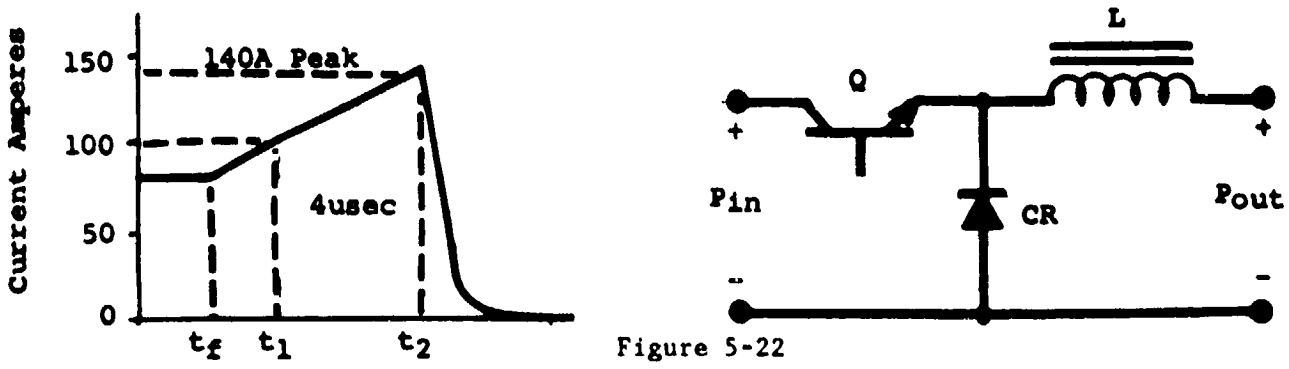


Figure 5-22

The estimated size and weight of this component is 2.5" x 2.3" x 2.1" and 1.71 pounds or 64 x 58 x 53 millimeters and .78 kilogram. The only advantage to be achieved with the electro-mechanical device is reduced switch drop. Typically, the power relay will achieve 150 millivolts drop coupled with 50-75 millivolts of inductor drop for a 200-225 millivolt switch drop. This is compared to the typical transistor saturation drop plus inductor drop of 200 + 100 or 300 millivolts.

A further power switch modification which can be used to either reduce the value of L or to eliminate it, would be to use di/dt control in the power switch circuit. This would be accomplished by minor loop feedback within the power switch and has been successfully applied for RPCs of ratings up to 20A at 28 VDC, 30A at 120 VDC, and 2A at 300 VDC. A signal proportional to load current for di/dt control of the main switch base drive can be obtained in a number of ways, two of which are:

1. emitter voltage degenerative feedback obtained by IR drop signal proportional to load current; and
2. base current degenerative feedback obtained electromagnetically from an inductor or transformer that carries load current. The limiting factor in this approach will be the 50A capability of the power switch transistors.

5.7.1.1 Conclusions and Recommendation

It must be recognized that the electro-mechanical and solid state switch hybrid is not a feasible approach when the source is a noncurrent limited or "stiff" source because of the extraordinarily large inductor required. Furthermore, the forward loss for the transistor can be made approximately the same as for an electro-mechanical type. The holding current for an electrically-held relay will be approximately the same as the control power loss for the transistorized solid state switch. The possibility of using a magnetically-held relay will reduce these control losses at the price of greater complexity, but will not overcome the basic problem of using an electro-mechanical relay to interrupt current from a noncurrent limited source. Therefore, the recommendation for noncurrent limited sources is to use power transistors for the power switching element.

5.7.2 Solid State Switch Circuit Considerations

Since the source is in reality a stiff (noncurrent limited) source, several problems result with the switching transistor: (1) the loads on the output of the static switch will in some cases contain filter capacitance on their input, and (2) faults in the load bus require an isolating impedance to safely ensure that the transistor switch can be turned off before excessive current is passed through the switch. (This results from carrier storage within the transistor.)

5.7.2 Solid State Switch Circuit Considerations (Continued)

Condition 1 imposes a very low impedance on the switch at "turn-on". A limiting means must be employed for safe operation. This is especially true for the triple-diffused type transistors, which will be employed for safe operation. Also, the typical load capacitance value that may be present is not known .

Condition 2 becomes a necessity in view of the fact that the transistor switch is driven into hard saturation during the "ON" time to keep forward losses (Vce) low. When a transistor is driven into hard saturation, carriers are present in the base-emitter junction which maintain the transistor "ON" after the base drive is removed. This is termed storage time for a device. In addition to the storage time, the transistor has a finite switching time.

Therefore, there is need for an isolating impedance to limit the peak current in the switch which will continue to increase after a fault occurs, even though the base drive is removed. This impedance is depicted as L1 in the HVDC solid state switch functional diagram, shown in Figure 5-23, and the following paragraphs describe important circuit parameters.

5.7.2.1 Determination of Series Inductance

The minimum amount of series output inductance (L1) required is determined by the storage and fall times of the particular transistor used as the power switch. Because the load current passes through it, it represents an additional series drop and thus has watts loss associated with it. The watts loss is inversely proportional to the weight, which results in a trade-off.

The sizing of this inductor is based on the following requirements:

1. Sensing circuit detects at 100 amperes and removes base drive.
2. I peak will be allowed to be 140 amperes.
3. Voltage applied maximum and worst case is 500 volts.

Utilizing the basic relationship $e = L(di/dt)$ we can solve for the required inductance, for a ΔI of 40 amperes. The inductance required for each microsecond of storage and fall time is:

$$L_i = e\frac{\Delta t}{\Delta I} = \frac{(500V)\ (1 \times 10^{-6}\ \text{sec.})}{40\ \text{Amp,}}$$

$$L_i = 12.5 \times 10^{-6} H \text{ per microsecond of storage and switching time.}$$

A tabulation of required inductance as affected by power switch shut-off time is shown in Table 5-3, while Table 5-4 shows the relationship of inductance, losses, and weight.

5.7.2.1 Determination of Series Inductance (Continued)

Table 5-3

Power Switch Operating Time Vs. L1 Requirement

$t_{stg} + t_f$ (μsec.)	1	2	3	4	5	6	7	8
L1 (μH)	12.5	25.0	37.5	50.0	62.5	75.0	87.5	100.0

Table 5-4

Series Inductance Vs. Losses/Weight

Inductance	Losses (Watts)	Weight (Pounds/Kg.)					
		CU		FE		TOTAL	
		Lbs.	Kg.	Lbs.	Kg.	Lbs.	Kg.
50 μH	4	0.93	0.42	1.67	0.76	2.60	1.18
	8	0.59	0.35	1.12	0.51	1.71	0.78
	16	0.35	0.16	0.75	0.34	1.10	0.50
62.5 μH	4	1.13	0.51	2.19	0.99	3.32	1.51
	8	0.76	0.34	1.46	0.66	2.22	1.01
	16	0.47	0.21	0.98	0.44	1.45	0.66
80 μH	4	1.48	0.67	3.02	1.37	4.50	2.04
	8	1.04	0.47	1.86	0.84	2.90	1.32
	16	0.58	0.26	1.30	0.59	1.88	0.85
100 μH	4	2.03	0.92	3.68	1.67	5.71	2.59
	8	1.24	0.56	2.47	1.12	3.71	1.68
	16	0.80	0.36	1.67	0.76	2.47	1.12

5.7.2.2 Input Capacitance Determination

The power switch circuit of Figure 5-23 utilizes an input capacitor, C1, whose purpose is to provide a sink for the energy stored in the line and source inductances that feed the solid state switch. The table below shows the input capacitor (C1) requirements for the solid state switch as a function of this line and source inductance. C1 is selected such that the voltage step produced will be limited to 20 volts at an input of 500 volts, and with a peak current in the input lines of 140 amperes.

Source Inductance	Input Filter Capacitor (C1)
10 μH	10 μF
20 μH	20 μF
30 μH	30 μF

*C1 is determined by the relationship $\frac{1}{2} LI^2 = \frac{1}{2} CE^2$

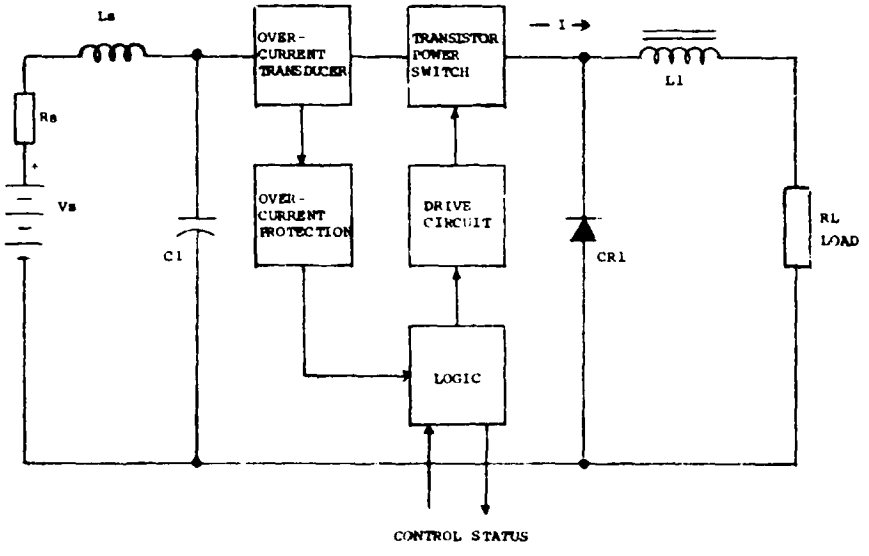


Figure 5-23

HVDC SSSW Functional Diagram

5.7.2.2 Input Capacitance Determination (Continued)

The results show a quite linear relationship that requires 1 microfarad for each microhenry of source inductance.

In considering likely values of source inductance, both the power supply and the feeder lines should be considered. The S.O.W. defines the applicable sources as solar arrays and DC-DC inverters; feeders are assumed to be at the most approximately 20 feet (6.1 meters) of #8 wire.

For solar arrays, a source impedance that is capacitive and resistive is presented by the semiconductor constituency of the array. Therefore, no inductance is attributed to array-type sources.

For DC-DC inverters, many circuit permutations are possible when considering the possible methods of filtering, regulation, and limiting which affect the transient and overload behavior as well as output transfer characteristics. For this analysis, inverter sources will be assumed to have non-inductive outputs, since specific definitions were lacking and since there is a greater probability of a capacitor output type filter.

5.7.2.2 Input Capacitance Determination (Continued)

In evaluating the impedance presented by the feeders, little can be defined at this time regarding configuration, relationship to a ground plane or pairing of the source and return leads. In addition, the impedance presented to a step wave front that would be encountered in event of a heavy fault would probably vary from the values obtained by DC or AC methods. However, in attempting to establish a measure or range of values, the following references were used:

1. From the I.E.E.E. Std 128-1976, Guide for Aircraft Missile Systems, the impedance at 400 Hz for #8 wire feeders would be:

$$Z_F = .7 + j\ .226 \text{ per } 1{,}000 \text{ feet } (.3 \text{ kilometer})$$

or

$$Z_F = .7 + jw\ (90 \times 10^{-6}) \text{ per } 1{,}000 \text{ feet } (.3 \text{ kilometer}).$$

For a 20 (6.1 meters) foot feeder:

$$R_{eff} = .014 \times 2 = .028 \text{ ohms},$$

$$L = 1.8 \times 2 = 3.6\ \mu H.$$

2. A classical analysis of a closely coupled #8 pair with 1/16th (1.6 millimeters) thick insulation gives .2 μH per foot (.3 meter). Twenty feet (6.1 meters), then, of this would result in 4 μH inductance.

5.7.2.2 Input Capacitance Determination (Continued)

3. From Reference Data for Radio Engineers, for telephone line pairs at 100 Hz:

$$Z = 6.82 + jw\ 3.53 \text{ per mile (1.6 kilometers).}$$

For a 20 (6.1 meters) foot feeder:

$$R_{eff} = .026 \text{ ohms,}$$

$$L = 13\ \mu H.$$

4. And from wire tables, for #8 wire:

$$R_{DC} = .628 \text{ ohms per 1,000 feet (.3 kilometer)}$$

or

for a 20 (6.1 meters) foot feeder:

$$R_{DC} = .628 \times 40/1000 = .025 \text{ ohms.}$$

On this basis, for the power sources and feeders being considered the source impedance range is approximated at:

$$R_s = .025 \text{ ohms minimum,}$$

$$L_s = 4\text{-}15\ \mu H.$$

With these values, the value of C1 would correspondingly range from 4 μF to 15 μF.

5.7.3 Further Trade-Off Considerations

As discussed in Section 5.7.1, it was determined that with high current capability sources, an electro-mechanical switch was impractical because its slow operating speed required an excessively large current limiting inductor.

The use of state-of-the-art devices in a "most likely to succeed" circuit approach also fell short of performance goals. Reflecting upon these discrepancies, it is concluded that some of the performance requirements impose constraints that are inconsistent with present devices and technology. For instance, the requirement for 200-500V operation, .2V maximum switch drop and 20W maximum dissipation at 80 amperes is not realizable with available or soon to be available power transistors. The additional IR drop of the fault current limiting inductor pushes the switch drop and losses further beyond limits.

In considering the next step, two different applications were considered that could be served by separate implementations. One application is with soft sources in which efforts to achieve low switch drop and low power losses are paramount. The other application is for hard sources, but the switch drop and power losses are not as critical and can be evaluated on the basis of a watts/pound trade-off.

5.7.3 Further Trade-Off Considerations (Continued)

The embodiment of a high efficiency device for use with soft sources can readily be accomplished in the electro-mechanical breaker form described in Section 5.7.1, without inductor, but with solid state turn-off circuitry.

Considering switchgear for stiff source applications, it would be worthwhile to review the performance requirements from the viewpoint of solid state implementation. The following analysis considers changes that could be made in solid state switch (SSSW) performance requirements resulting in improvements in areas of design difficulties, circuit complexity, unit size, and weight.

5.7.3.1 Switch Voltage Drop and Dissipation

The .2V maximum switch voltage drop along with the 20W maximum dissipation are undoubtedly the most difficult requirements to meet. Considering the .2V switch voltage drop, the following are compounding factors that make meeting this requirement herculean:

1. To meet .2V saturation voltage at 80 amperes, three to four large power transistors or many smaller devices must be paralleled.
2. The ballast inductor's IR drop adds to the switch drop, obtaining .05V drop at rated current results in an inductor weight of 2.6 pounds (1.2 kilograms).

5.7.3.1 Switch Voltage Drop and Dissipation (Continued)

3. The need to provide overcurrent protection requires the use of a current-to-voltage transducer, which in its simplest form is a resistive element that adds another .05V drop at rated current. This voltage drop could be reduced at the expense of circuit complexity with a current transformer approach (i.e., transductor), but this is not recommended.

From the standpoint of switch voltage drop itself, the value of .2V compared to 1.0V or 2.0V is insignificant at the voltage levels being considered. However, the dissipation due to the switch drop is the major loss in the SSSW and would increase from 16W at $.2V_{sw}$ to 80W at $1.0V_{sw}$ and 160W at $2.0V_{sw}$ at rated load current (80 amperes).

If the allowable switch voltage drop was considered on the basis of being within the confines of meeting a specified SSSW efficiency, perhaps a more amiable solution could be obtained. Considering nominal bus voltage, 300 VDC, the relationship between the allowed power loss and the maximum switch drop voltage is shown in Figure 5-24.

Of significance is the feasibility of using Darlington configurations in the power switch if the allowable power loss is in the vicinity of .5 to .75%. The use of the Darlington power stage offers the following advantages:

1. Reduction of drive power requirements by a factor of about ten per stage, simplifying the drive circuit and lowering its power level.

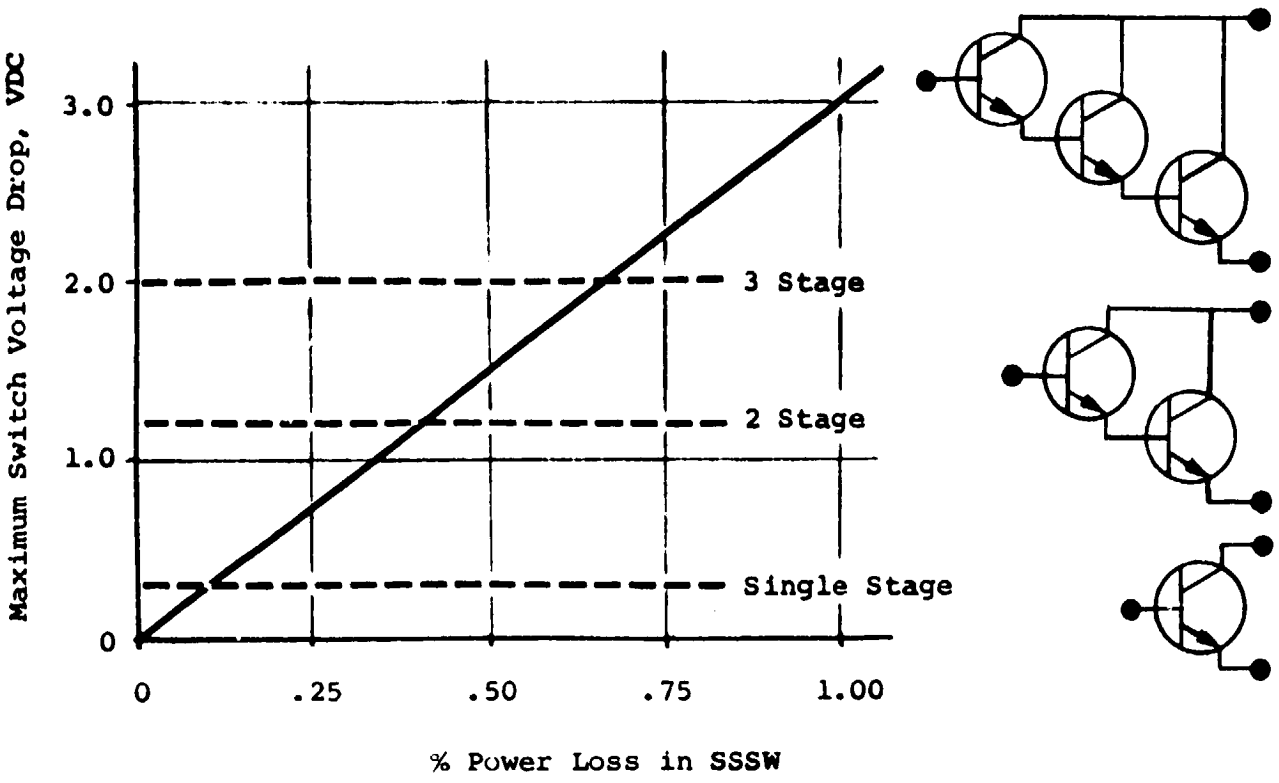


Figure 5-24

Effect of SSSW Loss Allocation Vs. Maximum Permissible Switch Drop Voltage

2. The potential of eliminating transformers from the drive circuit and thereby their associated size and weight.

3. The possibility of performing "active" di/dt control, thereby either significantly reducing or eliminating the fault current limiting inductor.

4. Improved SSSW dissipation at no load and light loads since the drive power is significantly reduced; consequently, the continuous control power drain will also be lower.

5.7.3.2 Current Rating

The considerations for current rating are twofold: rated and the interrupt peak values. The rated value of current affects the power dissipation in the SSSW while the interrupt peak current represents the short-term capability that must be designed into the

5.7.3.2 Current Rating (Continued)

power stage. Generally, any reduction in the 80A rating would be beneficial. A rating of 50A has been suggested by NASA as an acceptable continuous rating. This will reduce power levels and dissipations proportionally in the power and drive stages.

Considering the peak interrupt current value, the corresponding value for the 50A rating would be $\frac{50}{80}$ x 140 or 87.5 amperes. Considering this peak level, either one or two D60T type devices as the output element are feasible, offering simplification, size, and weight benefits.

5.7.3.3 Voltage Rating Considerations

The specified operating voltages are:

Rated Operating: 300 $\pm$ 100 VDC

Total Operating: 200 to 500 VDC

In the selection of power transistors the requirement to operate with potentials of up to 500V led to the selection of 600V devices. As a trade-off: if the interpretation of the operating limit is such as to consider the band from 400 to 500 VDC as a transient voltage region and if OV protection could be performed within the SSSW at and slightly below the 500V, then there would be two opportune possibilities:

1. There are more transistors available in the 500-550V_{ceo} class than in the 600V_{ce} class, some offering significant size/weight savings.

5.7.3.3 Voltage Rating Considerations

2. The value of the input capacitor, C1, was determined upon the basis of being able to absorb the energy kicked back from the source-feeder inductance when a heavy fault is cleared. The energy to be dissipated in this condition for 80A peak and 10 μH is not excessive, .032 joules, and is well within the capability of varistors and Zener diodes. Also, it is felt that varistors and Zener diodes will provide more positive protection for the SSSW as they operate at or become active at a designed threshold/protection level, whereas a capacitor would be entirely passive and offer no degree of protection beyond for spike voltages and short-term transients.

5.7.3.4 Active di/dt Considerations

The inclusion of L1 was to preclude the excessive fault current levels that could occur at power switch turn-off. The 50 μH value was predicated upon limiting the peak short circuit current to 140 amperes with a 4 μsecond turn-off time and a 500 VDC source. While L1 has the attribute of providing "saving grace" in event of a severe output fault, it has a number of abominable effects:

1. its IR drop adds to the switch voltage drop;
2. it is a sizeable and weighty component;
3. it adds turn-off duress to the power switch by virtue of assuring inductive turn-off conditions; and

5.7.3.4 Active di/dt Considerations (Continued)

4. the value of "L" selected only meets the situation for maximum transistor turn-off time (4 μseconds), maximum supply voltage (500V) and the desired value of peak fault current (140A).

However, at 400 VDC the maximum value of load capacitance without causing an overcurrent protection trip-off would be only about 2 μF.

If active instead of reactive, di/dt load current control is employed by using minor-loop feedback in the power switch; these detriments could be for the most part surmounted. This technique was successfully employed in the previous RPC development programs and is feasible only in the Darlington power switch configuration because analog control during switching operations can only be accomplished in driver stages without incurring the risk of power switch secondary breakdowns. For a reference, the 30A/120 VDC RPC had a short circuit response of about 90A peak in 230 μseconds, while the 2A/300 VDC RPC had a 12A peak in 145 μseconds. For this application, a good beginning would be an 80A peak in 100 μseconds based upon:

1. an instant trip level about 175% of rated; and
2. an overload persistance that allows almost full voltage, full current utilization of the power switch transistors without exceeding their SOA capabilities.

With these values, an anticipated load capacitance of 10 μF. can be handled without causing inrush overcurrent trip-offs. From the original design, this represents a fivefold increase in inrush capacity with the SSSW acting as a softer charging source.

5.7.3.5 dv/dt Considerations

Finally, dv/dt is a consideration in that it is a consequence of the performance of the SSSW with inductances in the power circuit path. One important function of the SSSW is that of an interface: it determines how the load appears to the source and vice versa. If the SSSW exerts an inertial effect upon current transistions (i.e., load switching and fault removal), then to both load and source this also provides dv/dt benefits. Allowing reactive energy to be dissipated at a smoother rate will help make the overshoots and inrushes more benign, uniform, and repetitive while hopefully precluding the need for a power switch snubber that would be large in size and degrade SSSW reliability.

5.8 Recommendation

5.8.1 New Option Recommendation

It is recommended that a new option, designated as Option II, Type C, be considered with the following specifications:

Parameter	Limits
Rated Operating Voltage	200-400 VDC
Max. Transient	500 VDC
Source Current Capability	500 Amperes
Rated Output Current	50 Amperes
Interrupt Capacity	80 Amperes
Efficiency: Min.	99.0%
Objective	99.5%

5.8.2 Proposed Circuit

The HV SSPC circuit, shown in Figure 5-25, represents a uniting of the trade-off considerations in this section. Its specific objectives are the attainment of SSPC-like performance in the context of all specification relaxations being given. This is a circuit that was recommended and became the genesis of Task IV. It is based upon the established circuitry of the prior 120 VDC and 300 VDC programs.

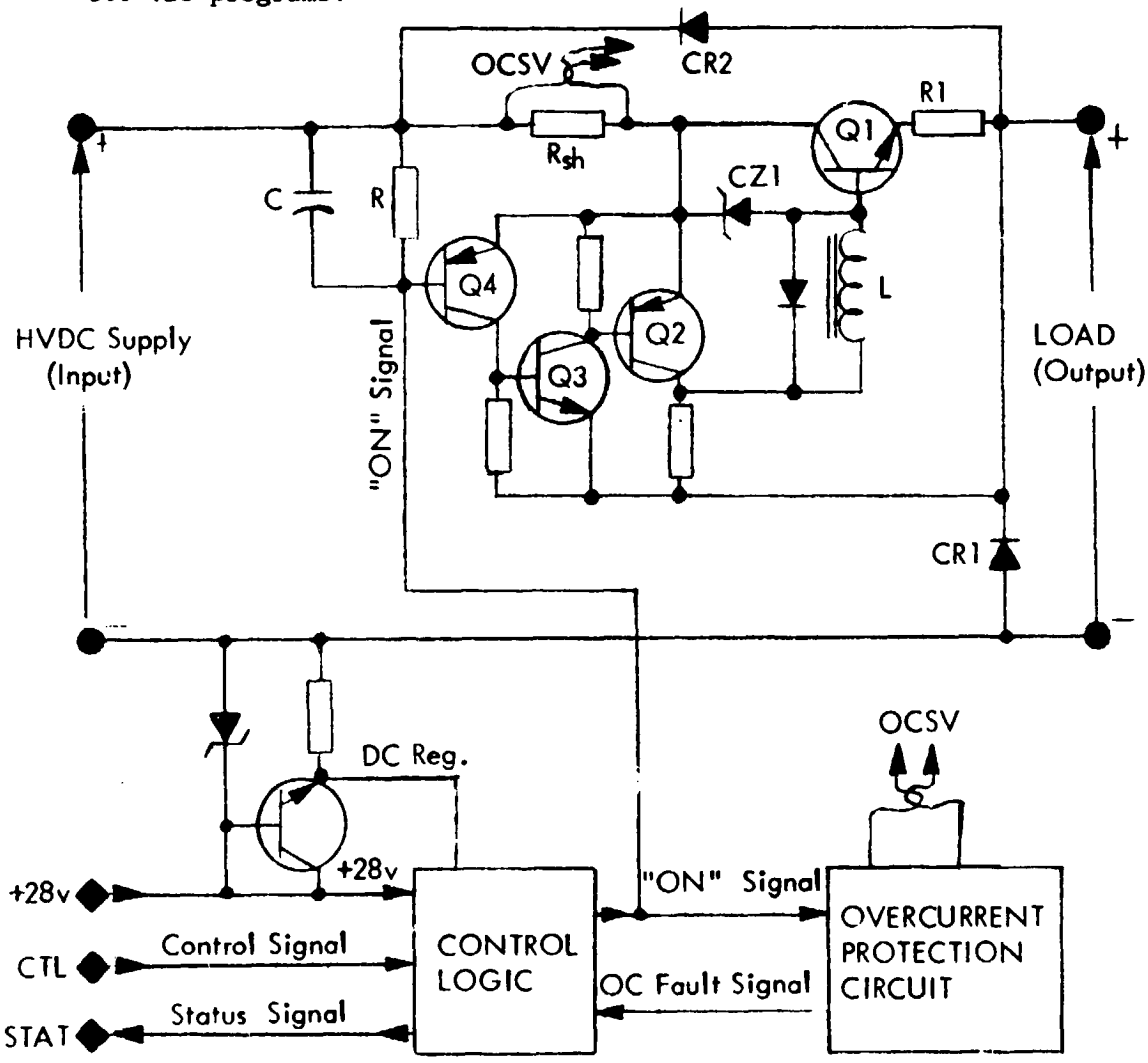


Figure 5-25

HVDC SSPC Functional Schematic

C - 2

SECTION VI

DESIGN AND FABRICATION (TASK IV)

6.1 Task Objectives

The objectives of Task IV, based on the results of Task III, were to formulate a maximum of two designs for each type of switchgear and build one breadboard model of each type.

6.2 Synopsis

The purpose of this task was to design and evaluate suitable circuit approaches to meet the performance specifications that were formulated in Task III. The first specification is for an 80A/200-400 VDC latching-type relay with solid state commutation, whereas the second is for a 50A/200-400 VDC SSPC. This section includes circuit descriptions for these two HVDC switchgear designs that were evaluated in Task V. Design specifications D-774147 and D-774149 for these devices are included in Appendix B and C respectively.

6.3 80A/400 VDC EM/SSCB

The goal is to develop a circuit breaker for HVDC applications that utilizes a solid state arc extinguishing circuit (i.e., current commutation) that will provide the desired physical size advantages along with operational and reliability benefits. The critical performance parameter requirements are:

Operating Voltage	200-400 VDC
Rated Current	80A
Max. Interrupt Current	100A
Max. Contact Drop	.20 V at 80A
Operating Mechanism	Latch-Type
Weight Objective	3.5 Lbs* (1.6 kg)

*Actual unit weight achieved was 3.05 Lbs (1.4 kg).

6.3.1 Circuit and Semiconductor Considerations

There are two types of solid state power devices that can provide 400V/100A interrupt capability as required: SCR or transistors. As shown in Table 6-1, the advantages of the SCR outweigh those of the transistor. However, the current turn-off of SCRs in DC circuits is difficult, but it can be accomplished in two ways:

1. reverse gate turn-off devices; and
2. L-C commutation.

Table 6-1

SCR/Transistor Comparison

Comparative Rating

Parameter	SCR	Transistor
Power Gain	High	Low
Device Size & Weight	Small	Large
Voltage Capability	High	Fair
Current Capability	High	Low
Turn-off in DC Circuits	Difficult	Easy

Considering SCRs, the GTO (gate turn-off) device availability technology is not considered as "arrived" yet, and therefore, not worthy of serious consideration for this application. The L-C commutation approach has been proven, but is incapable of meeting the weight objectives due to the weight of commutation circuit components required.

Consequently, the solid state power device selected was a silicon power transistor which presently is available with the capabilities of reliable switching in 400 VDC/100A circuits.

6.3.1 Circuit and Semiconductor Considerations (Continued)

A second significant decision to be made regarded the means of actuating the transistor commutation circuit. Possible methods are:

1. signals derived from close and trip input signals;
2. arc sensing detection; and
3. auxiliary contact actuation.

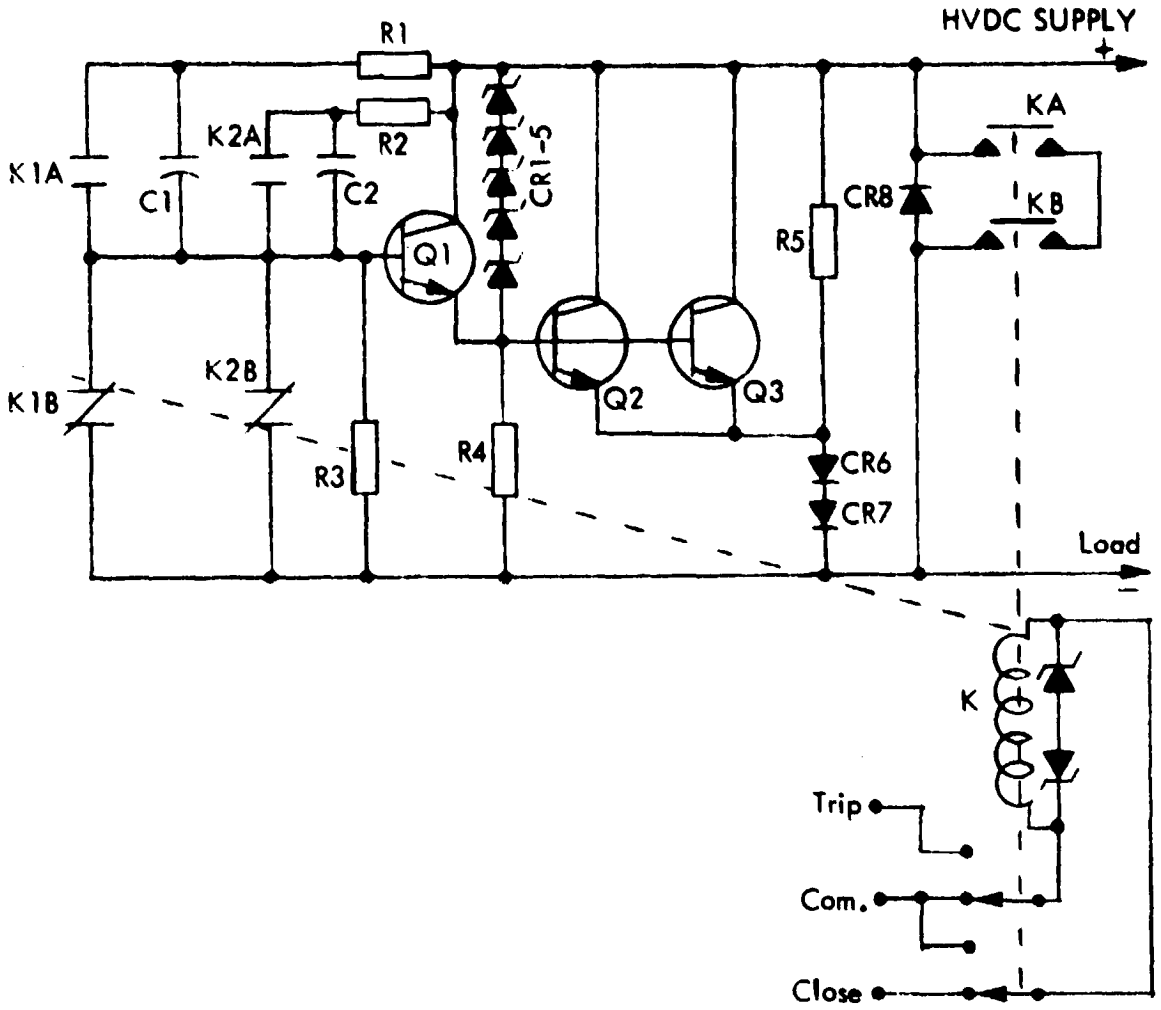
Of these possible methods, the third was selected on the basis of offering the least complex circuit approach and availability.

6.3.2 Circuit Description

The circuit diagram, Figure 6-1, shows the circuit which evolved for implementation into the prototype devices that were assembled and tested. The transistor stage is an NPN Darlington configuration utilizing three 500V/50A devices, one transistor (Q1) driving two transistors (Q2 and Q3) in parallel.

The input signal to Q1 is obtained from the parallel circuit paths consisting of R1-C1-K1A and R2-C2-K2A. K1 and K2 are auxiliary contacts that operate in synchronization with the power contacts, KA and KB, which are connected in series.

To understand circuit operation, assume the circuit breaker is in the open state; that is, KA, KB, K1A, and K2A are open. Q1, Q2, and Q3 are nonconductive and a small bleeder current flows through R5, CR6, and CR7, due to the open circuit potential drop (VDC) across KA and KB. This causes a reverse bias voltage in the Q2-Q3 base-emitter circuit that enhances the transistor's blocking voltage. Contacts K1B and K2B are closed, shorting the Q1 base to improve its voltage blocking capability.



Ckt. Des.	Description	Part Number
C1, 2	.01 µF/1000V	Semtech Type SCR or Equivalent
CR1-5	100V/5W	1N5378B
CR6-8	600V/6A	Material Type MR756
K	Ckt. Bkr.	W AVB-236A
Q1-3	500V/50	Solitron Type SDT55472 or Equivalent
R1, 2	100 /.5W	RC20GF101J
R3, 4	1K/.25W	RC07GF102J
R5	150K/1W	RC32GF154J

Figure 6-1

AVC-41 EM/SSCB Circuit Diagram

6.3.2 Circuit Description (Continued)

If the circuit breaker is subsequently operated by applying a close signal to its coil, the NO main and auxiliary contacts will move into their closed position. The auxiliaries typically operate a millisecond later than the main contacts in closing, so that the main contact will establish the current flow from source to load. With the main contact closed, the transistor circuit is effectively shorted out. However, the bouncing of the main contacts immediately after closing that would normally result in arcing is effectively clamped out by the transistor commutation circuit. When K1A and K2A are closed and a voltage potential across the main contacts, as occurs with contact bounce, current flows through R1 and R2 into the Q1 base, causing Q2 and Q3 conduction and clamping of the power contact drop to about 25 VDC (see switch voltage waveform pictures for closing, the .5-1 milliseconds immediately after contact closure).

6.3.2 Circuit Description (Continued)

When the breaker is opened, the transistor circuit "assists" the circuit breaker in a soft turn-off commutation that occurs in the following manner. In opening, the auxiliary contacts K1A and K2A lag, timewise, the main contact opening on the order of 1 millisecond. Consequently, as the main contacts (KA and KB) open, the potential buildup across them for this 1 millisecond period results in base drive to Q1 and the conduction of the transistor switch and the transfer of load current from the metal contacts to the transistors. This results in the elimination of arcing while the contacts open sufficiently to block the full HVDC potential. When the auxiliary contacts K1A and K2A open, base drive is removed from Q1 at a controlled di/dt rate determined by C1-R1, C2-R2, and circuit operating voltage. This results in a "soft" contact voltage rise across the circuit breaker contacts.

6.3.3 Reliability Analysis

A reliability stress analysis was performed on the AVC-41 EM/SSCB as it would be configured for a production version. This analysis was done by MIL-HDBK-217C procedures with the following ground rules and considerations:

1. environment = space fixed;
2. redundancy in the Zener diode string (CR1-5) and transistor drive circuits (R1-K1A and R2-K2A) was not considered in the analysis to provide conservative FR values;
3. transistor stresses are based on .1% duty-cycle at rated load;
4. the contactor FR is based on aircraft performance data; and
5. an ambient of 60°C was assumed as being typical for application.

Table 6-2

****
* E-M CKT BKR RELIABILITY ANALYSIS *
* MIL-HDBK-217C *
****

ITEM	NO.	TEMP	STRESS	F-RATE	TOTAL
RESISTOR-RCR	4	60	0.00	0.0000	0.0001
RESISTOR-RCR	2	60	0.40	0.0000	0.0001
CAPACITOR-CKR	2	60	0.30	0.0000	0.0001
TRANSISTOR-NPN	3	75	0.52	0.1571	0.4714
DIODE-SILICON	2	65	0.00	0.0051	0.0103
DIODE-ZENER	3	65	0.01	0.0116	0.0348
HAND SOLDER	29	60	0.00	0.0026	0.0754
RELAY	1	60	0.01	0.0028	0.0028
CONTACTOR	1	60	0.00	10.0000	10.0000
TOTAL FAILURE RATE MILLION HOURS					10.5949

****
*
* MTBF= 94385 HOURS *
*
****

6.4 50A/400 VDC SSPC Description

6.4.1 Circuit Objectives

The following criteria were established for circuit selection:

1. SSPC circuitry is to be based on proven circuits and concepts of the previous 120 VDC and 300 VDC programs.
2. Performance-wise, the SSPC should utilize instant trip-type overload protection and other functions as defined by D-774149.

6.4.2 SSPC Functions

Referring to the schematic diagram (ED 393830), the following functions are provided:

1. Control Functions
   a. Power Supply
   b. Control Switch Logic and Time Delay
   c. Power Ready
   d. Trip Lockout
   e. Drive Circuit
   f. Power Switch
2. Protection Functions
   a. Overcurrent
   b. 28 VDC Undervoltage
3. Indication Function
   a. Tripped Indication

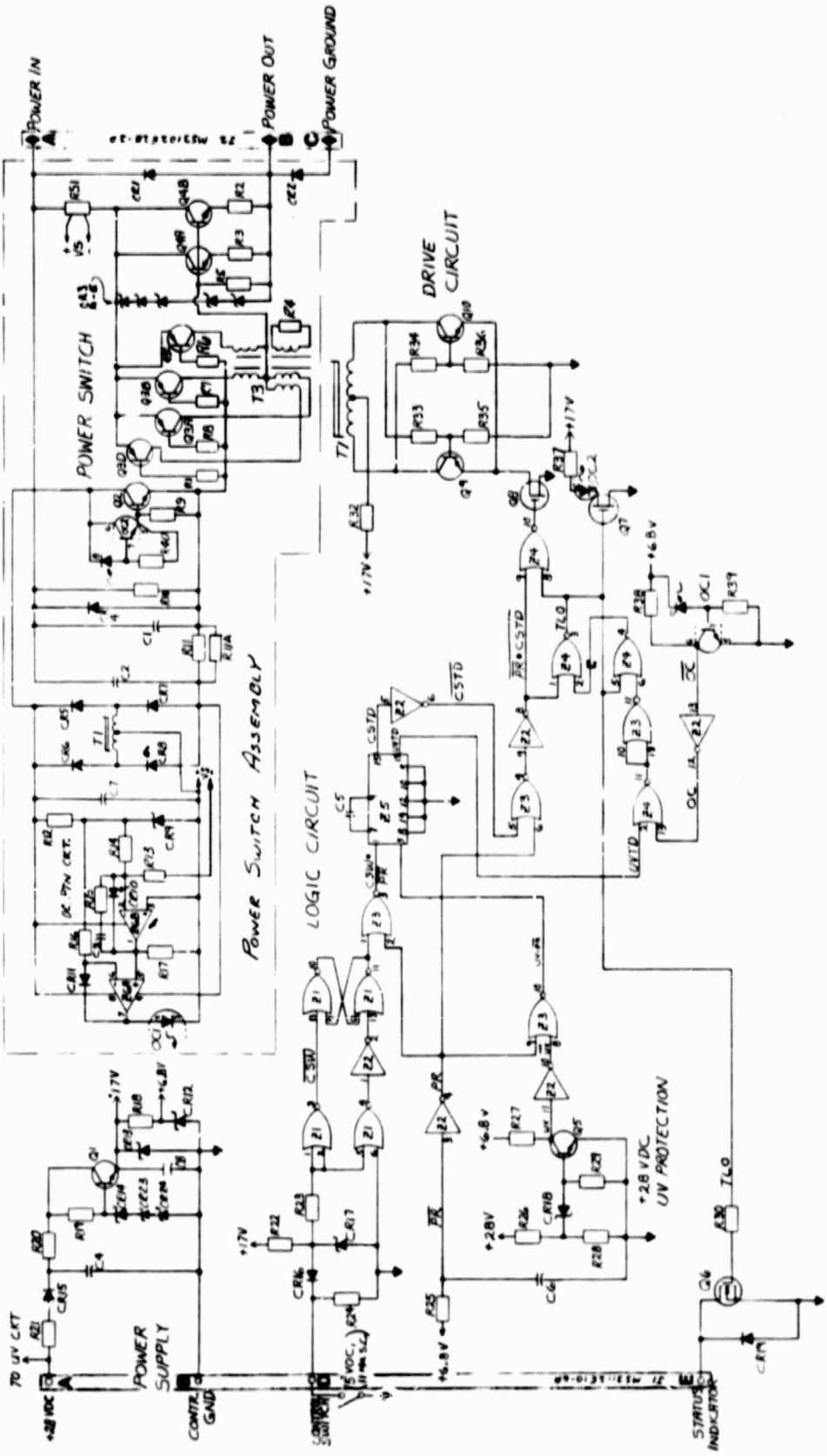


Figure 6-2

Schematic Diagram - 50A/200-400 VDC SSPC

Table 6-3

AVC-43 50A/200-400VDC SSPC (NASA-LEWIS) SCHEM. DGM. ED393830

ENGINEERING REFERENCE ONLY
DO NOT ORDER FROM THIS DRAWING

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION	
C06	CKR05BX683KP	CAPACITOR, CERAMIC	.068/50V WESTCAP
C01	906D715-14	CAP SOLID TANTALUM	3/01-2286 100 20VK
C04	906D715-19	CAP SOLID TANTALUM	3/01-2306 22U 35VK
C02	906D715-43	CAP SOLID TANTALUM	SP T110 1.0U 35VK
C07	906D715-46	CAP SOLID TANTALUM	SP T110 3.9U 35VK
C05	906D715-54	CAP SOLID TANTALUM	3/01-2314 4700P 35VK
C08	928A460-14	CAPACITOR, CERAMIC	CK06BX .47U 50VK
CR03,03,03,03,03	1N4981	DIODE,SI,ZENER	1N4981 82V
CR04,05,06,07,08,15, 16	927A496-2	DIODE,SI,FAST,REC	J4148 75V .1A 0035
CR01,02	932A362-4	RECTIFIER,SILICON	MR7566(3V 6A A264
CR19	932A736-1	DIODE,SILICON	JX486B 225V .1A DO7
CR13	938D392-11	DIODE,SI,ZENER	18V 5P-.05M.4W DO7
CR24	938D392-2	DIODE,SI,ZENER	3.3V 5P-44A.4W DO7
CR17	938D392-5	DIODE,SI,ZENER	5.6V 5P-1MA.4W DO7
CR12,14,23	938D392-6	DIODE,SI,ZENER	6.8V 5P-.5M.4W DO7
CR18	938D392-7	DIODE,SI,ZENER	8.2V5P-.05M.4W DO7
OC01,02	HP4351	OPTICAL COUPLER	HI-SPEED/145NW H-P
Q09,10	2N3700	TRANSISTOR, NPN	.5A/80VCEO TO18
Q06,07,08	2N6660	FIELD EFFECT TRAN	60V/1A TO-5 SCNK
Q01	929A091-2	TRANSISTOR, NPN,PWR	3441 140V 3A T066
Q02,05	932A729-1	TRANSISTOR, NPN	JX2219A 50V .8A TO5
Q03,03,03	MJ6503A	TRANSISTOR, PNP, PWR	500VCE B=30,IC=1 MTL
Q04,04	D60T	TRANSISTOR, NPN,PWR	400V/40A WESTINGHOUS
R02,03	*BALLAST-R	SPECIAL COMPONENT	EMIT'R-RSTR .05V/25A
R32	RCR20GF160J	RESISTOR CARB COMP.	16 T5 0.5W RCR20
R11,20	RCR20GF200J	RESISTOR CARB COMP.	20 T5 0.5W RCR20
R39,40	RC07GF205J	RESISTOR CARB COMP.	2.0M T5 .250W RC07
R09	18D3546-15	RESISTOR CARB COMP.	330 T5 .250W RC07
R22	18D3546-36	RESISTOR CARB COMP.	1.5K T5 .250W RC07
R06,07,08	18D3546-41	RESISTOR CARB COMP.	4.7 T10.250W RC07
R04,05	18D3546-44	RESISTOR CARB COMP.	100 T10 .250W RC07
R21	909C790-66	RESISTOR CARB COMP.	10 T5 0.5W RC20
R23	928A736-45	RESISTOR METAL FILM	49.9K T1 .125W RN60D
R25	928A736-60	RESISTOR METAL FILM	499K T1 .125W RN60D
R26,28	928A736-78	RESISTOR METAL FILM	20.0K T1 .125W RN60F
R24	932A720-10	RES.F.COMP .250W T5	RCR07G512JS 5.1 K
R10	932A720-14	RES.F.COMP .250W T5	RCR07G302JS 3.0 K
R19	932A720-15	RES.F.COMP .250W T5	RCR07G102JS 1.0 K
R30,38	932A720-16	RES.F.COMP .250W T5	RCR07G103JS 10. K
R27,29,35,36	932A720-22	RES.F.COMP .250W T5	RCR07G473JS 47. K
R33,34	932A720-40	RES.F.COMP .250W T5	RCR07G912JS 9.1 K
R37	932A720-75	RES.F.COMP .250W T5	RCR07G621JS 620.
R18	932A720-9	RES.F.COMP .250W T5	RCR07G202JS 2. K
RS1	*SHUNT-50A	SPECIAL COMPONENT	50MV/50A
R11	RCR20GF200J	RESISTOR CARB COMP.	20 T5 0.5W RCR20
T1	E393611	TRANSFORMER, MINIATR	PSW DR 200TCT-100TCT
T2	E393612	TRANSFORMER, PULSE	PSW PROT 20T-20T-20T
Z1,3,4	MC14001BAL	CMOS	QUAD2INNOR14001BAD14
Z2	MC14069BAL		CMOS HEX INVERTER
Z5	MC14490	CMOS	HEX CONT BOUNCE ELIM

* 200T #30 wire and 116T #28 wire on Magnetics, Inc. #80606-1A core.

** 20T trifilar on Magnetics, Inc. #55310-A2 core

6.4.3 Control Function Descriptions

6.4.3.1 Power Supply

The purpose of the power supply is to provide regulated DC voltages for the SSPC circuits. The 28 VDC supply voltage is regulated down to about 14 VDC by the CR14-23-24-25 string and Q1, and is maintained for 28 VDC supply variations ($\pm$7V). The CR-14-23-24-25 diode string provides temperature stability for the regulated voltage. The 6.8 volt regulated voltage is provided for the CMOS logic devices. CR13 provides protection against a component failure that could cause abnormally high regulated voltages, i.e., Q1 short, T1 secondary-primary short or CR14-23-24-25 open. Filtering is provided by C4 and associated components.

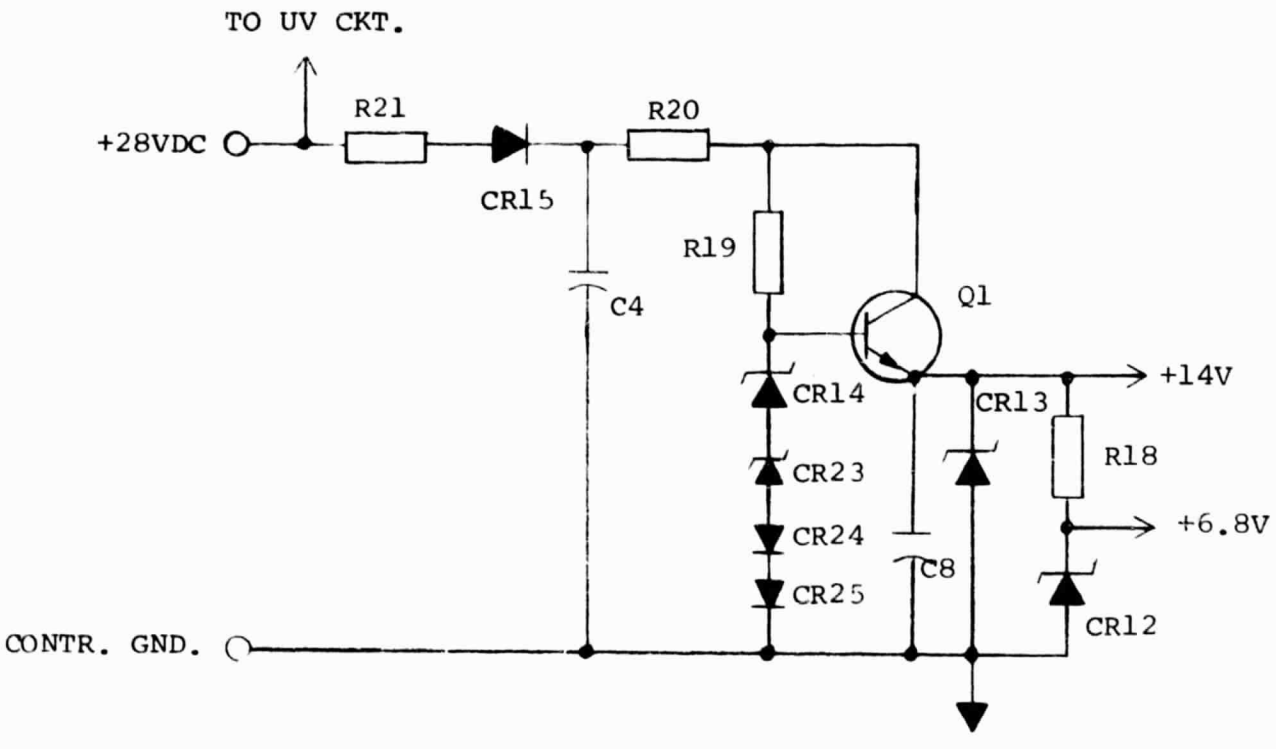


Figure 6-3

Power Supply Circuit

6.4.3.2 Control Switch Logic and Time Delay

The purposes of this circuit are to:

a. interface between the external SSPC OFF/ON control switch or signal; and

b. provide voltage hysteresis and time delay for operation stability.

As shown in the circuit diagram, the external control switch is a grounding device which when closed results in an "0" level signal at the control input and when opened results in a "1" level signal. The circuit is designed to operate with a TTL device in place of the switch. The control input voltage is applied to Gates Z1A and Z1B which operate as threshold detectors and to Z2A, Z1C, and Z1D which complete a toggle circuit. The circuit is designed to operate with a small amount of hysteresis (established by the Z1A and Z1B input connections) and provide a digital logic signal in response to the voltage level (CSW_{in}) at the control switch terminal. The output signal of Z1D, $\overline{CS}$, is high when the "CSW_{in} level is low and low when the "CSW_{in}" level is high. The "$\overline{CS}$" signal is gated with the Power Ready Signal (PR) so that the "$\overline{CS}$" signal only operates the Control Switch Time Delay (CSTD) when the PR signal is absent. The CSTD function is provided by Z5, a CMOS IC which is a digital time delay device of the contact bounce eliminator type. The CSTD period is on the order of 7 milliseconds, is a function of C5, and is provided for both turn-on and turn-off.

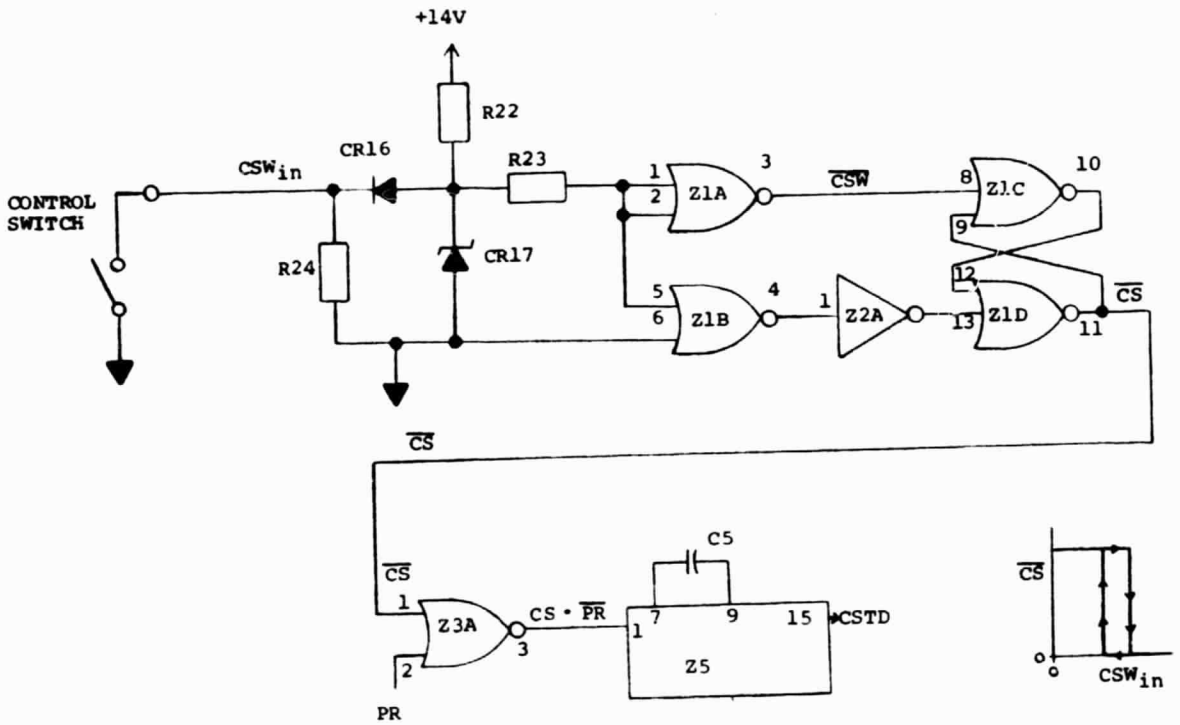


Figure 6-4

Control Switch Logic and Time Delay Circuit

6.4.3.3 Power Ready

The purpose of the Power Ready (PR) function is to initialize the SSPC logic circuitry when 28 VDC power is applied. This is accomplished in the PR circuit by an R-C time delay (R25-C6-Z2B) circuit which generates a pulse persisting for about 30 milliseconds when 28 VDC power is applied. This PR signal is utilized to lock out the undervoltage and control switch circuits and reset the control switch time delay and trip lockout circuits.

6.4.3.4 Trip Lockout

The Trip Lockout (TLO) function is utilized to provide trip-free operation for the prevention of SSPC OFF/ON cycling in the event of an overcurrent (OC) or an undervoltage (UV) trip-off. The TLO retention is provided by Z4A and Z4B which are connected to form a NOR flip-flop circuit. The PR and CSTD signals affect reset of the TLO circuit. The occurrence of an OC signal, via Optical Coupler OC1, or an undervoltage time delay (UVTD) signal causes the setting of the TLO circuit. The TLO signal is used to.

a. clamp the drive circuit via OC2;

b. de-energize the drive oscillator circuit; and

c. activate the status indication circuit.

Once the TLO circuit is set, it can be reset by closing and then reopening the control switch or removing and reapplying the 28 VDC power.

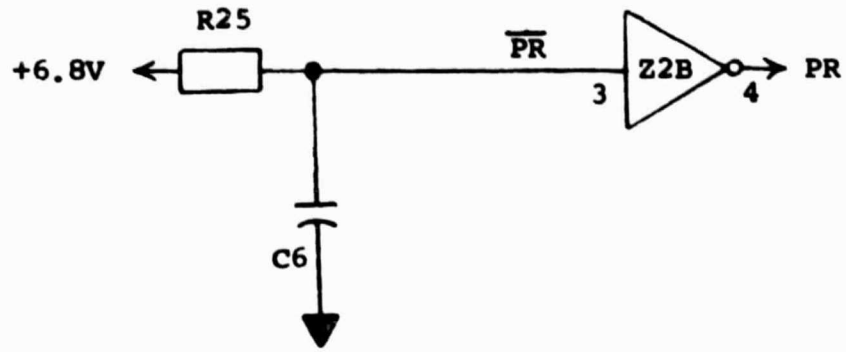


Figure 6-5

Power Ready Circuit

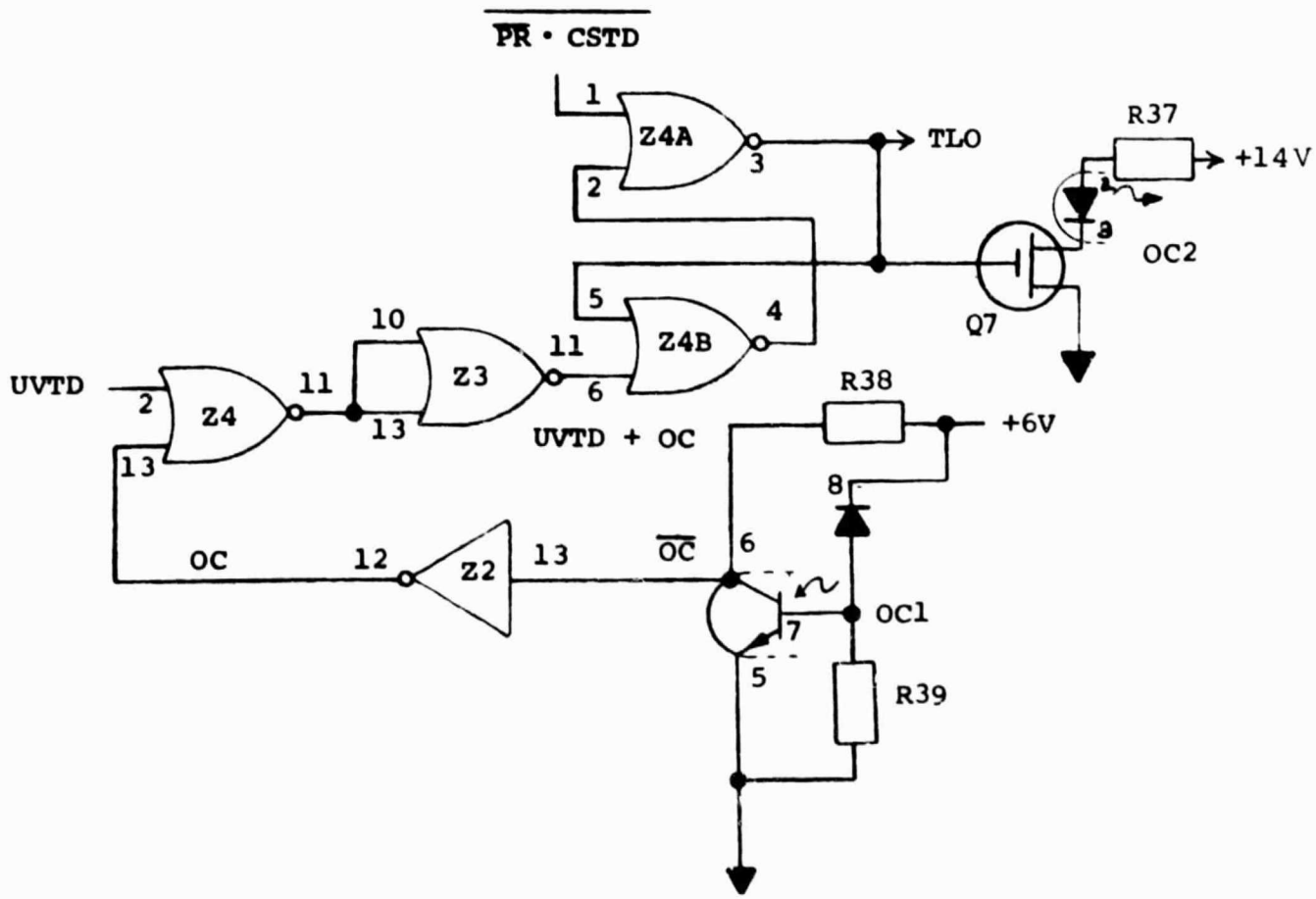


Figure 6-6

Trip Lockout Circuit

6.4.3.5 Drive Circuit

The purpose of the drive circuit is to provide amplification and electrical isolation for the logic "ON" signal which becomes the input drive signal to the power switch. The ON signal occurs when the CSTD signal is present and the PR and TLO signals are absent. The ON signal is amplified by Field Effect Transistor, Q8, which provides the grounding path for the Royer oscillator comprised of T1, Q9, Q10, and associated components. The secondary of T1 is full-wave rectified by CR5 through CR8 to provide positive and negative voltages which provide base drive to the power switch and energize the overcurrent protection circuit.

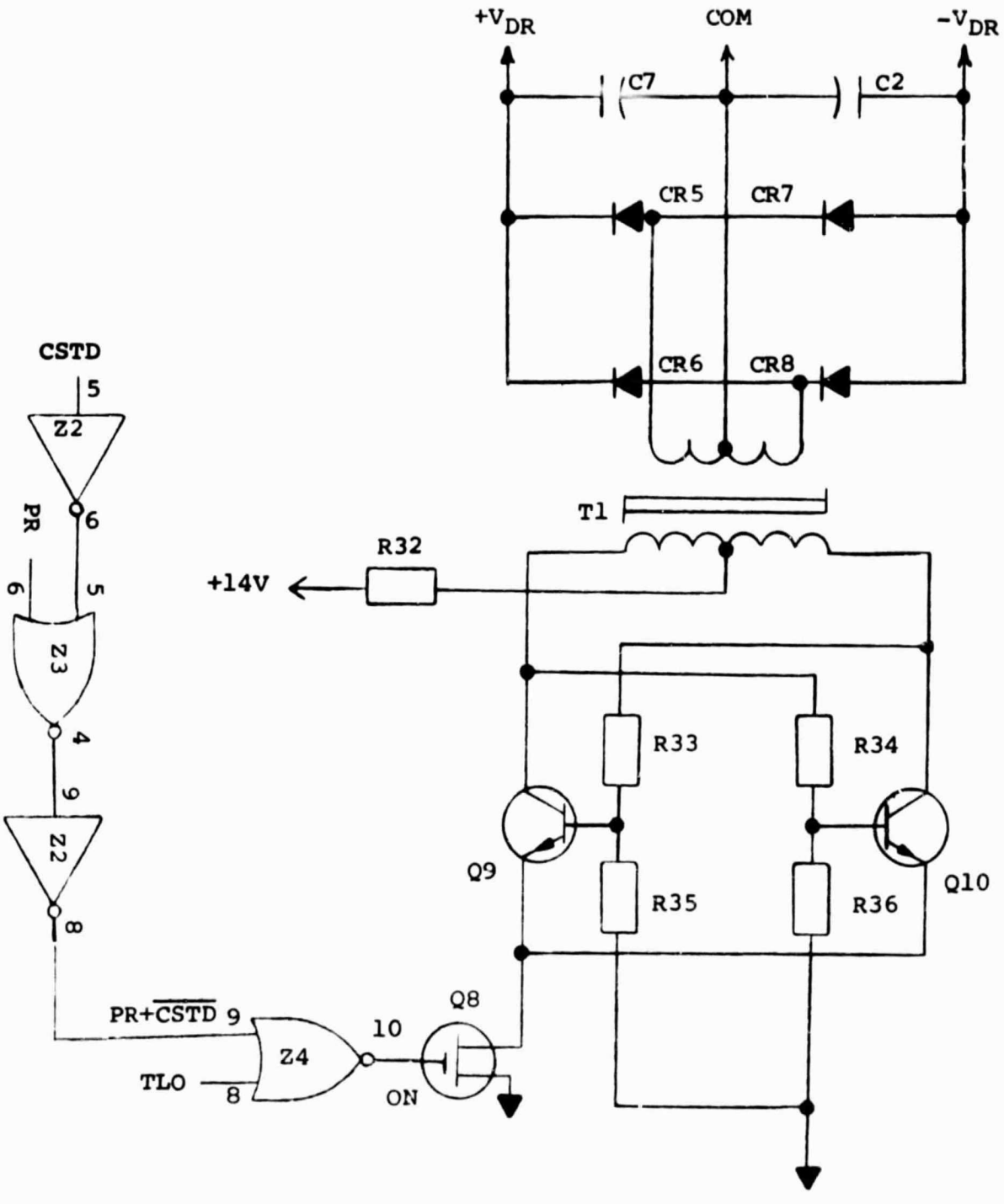


Figure 6-7

Drive Circuit, High Voltage DC, Solid State Power Controller

6.4.3.6 Power Switch

The power switch consists of Power Transistors Q3A through Q4B and associated parts. This PNP-NPN configuration is known as the complimentary Darlington type circuit. As shown, three paralleled PNP transistors drive two paralleled NPN transistors to provide the necessary power handling ability. T2 is connected between the PNP driver and the NPN output transistors and an isolated winding has R4 as a load. The purpose of T2 is to provide dynamic current limiting to protect the power switch and limit peak let-through currents during load transient and short circuit conditions. High voltage transient protection is provided for the power switch by the string of Zener Diodes CR3A-CR3E, which will break down for power switch voltages exceeding 450 volts. Power switch and load commutation is provided for by Rectifiers CR1 and CR2. A small voltage proportional to the load current amplitude is provided by RS1 for the overcurrent protection circuit.

The power switch is turned on by the drive circuit whose negative DC output voltage, $-V_{DR}$, is applied as base signals to the Q3A, B, and C through R11, R6, R7, and R8. Consequently, wherever the drive circuit is energized, base drive is applied to the input stage of the power switch to turn it on and apply the DC supply voltage to the load. Shaping of load current rise and fall at turn-on and turn-off is provided by the feedback loop comprised of the power stage, RS1, R10, and C1. This shaping provides soft-action in power switching operations and effective di/dt control which reduces the load switching transient voltage effect caused by inductance in the power circuit.

6.4.3.6 Power Switch (Continued)

The circuit consisting of OC2 and Q2 is utilized to clamp out the base drive to the power stage when an overcurrent trip-off occurs. This is necessary to limit the peak current amplitude which occurs under short circuit conditions.

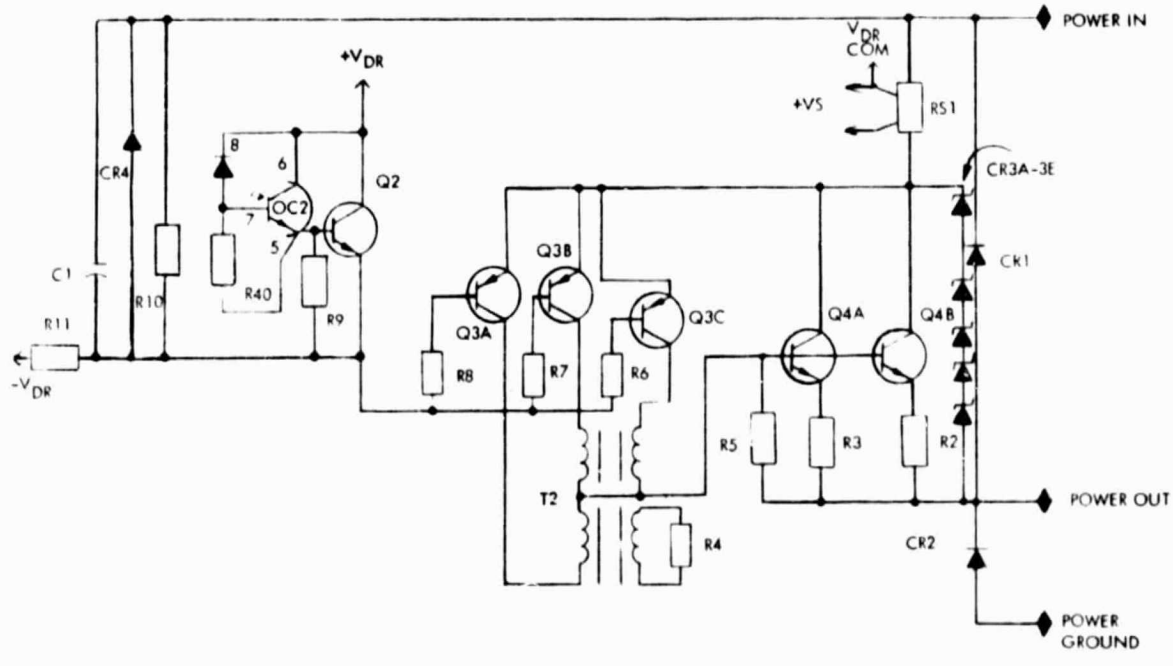


Figure 6-8

Power Switch Circuit

6.4.4 Protection Function Descriptions

Overcurrent Protection

The overcurrent protection circuit consists of Operational Amplifiers Z6A, Z6B, and associated components. Its purpose is to monitor load current and to provide a trip signal whenever the current level exceeds the minimum overcurrent threshold level, nominally about 1.25 per unit (P.U.) or 62.5 amperes. The tripping time is inversely related to the level of overcurrent; that is, the greater the level the shorter the tripping time. The overcurrent circuit functions in the following manner.

The V_S sensing voltage, proportional to the load current level, is applied as the input signal to Z6B via R13, and compared to a stable reference signal provided by CR9, R12, and R14. This reference signal is designed so that overcurrent tripping will not occur for load currents below the 1.25 pu minimum pickup level. However, for load current levels above this, Z6B performs as an integrator, i.e.: the Z6B output voltage at Pin 1 increases at a rate proportional to the amount of load current excess over the operating level and the circuit RC time constant of R13, R15, and C3. Current-time performance limits for this circuit are shown on Page A-12 of the Appendix.

The output voltage level of Z6B is sensed by Z6A (Pin 5), which functions as a comparator. When the Z6B output voltage exceeds the CR9 voltage level (at Pin 6 of Z6A), the Z6A output goes positive, driving the LED input of Optical Coupler OC1, which propagates the OC trip signal into the logic circuit causing SSPC trip-off and setting of the trip lockout.

6.4.4 Protection Function Descriptions (Continued)

The overcurrent circuit is energized by the $+V_{DR}$ and $-V_{DR}$ voltages obtained from the drive circuit. Consequently, this circuit is only energized when the SSPC is in the ON state. The circuit has been designed to provide almost instantaneous tripping in the event of short circuits, even in the event of turning on into a short circuit. Diodes CR10 and CR11 are incorporated into this circuit to improve the operational speed of Z6A and Z6B by maintaining their output voltages, within one diode voltage drop of their input voltage thereby precluding saturation mode operation.

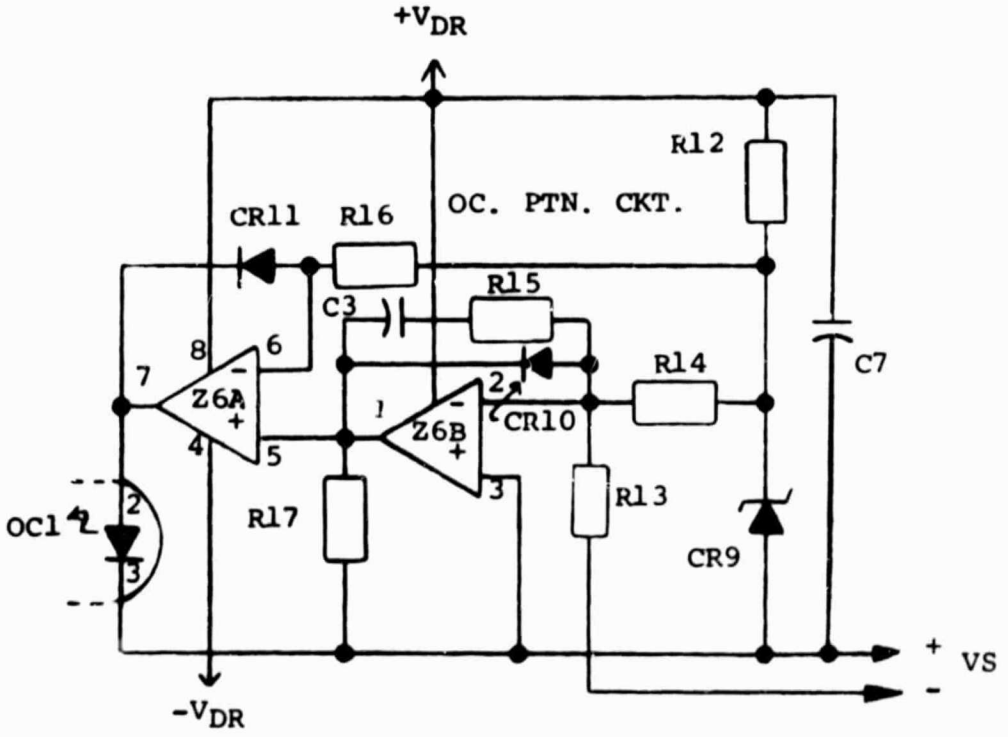


Figure 6-9

Overcurrent Protection Circuit

6.4.4.2 28 VDC Undervoltage Protection Circuit

The purpose of this circuit is to protect the SSPC in event the 28 VDC supply voltage becomes excessively low. This protection is necessary because the 28 VDC supply is used to power the drive circuit and when the 28 VDC supply drops below its 21 volt lower limit, drive to the power switch will be reduced, thereby risking excessive switch voltage drop and power dissipation.

The input to the 28 VDC UV circuit is the 28 VDC supply voltage, which is applied via R27 and CR18 to the Q5 base. When the 28 VDC supply voltage is above 21 volts, CR18 is broken down so that a base signal is applied to Q5 and Q5 is in the conducting state and its collector voltage is at a low potential. Whenever the 28 VDC drops below the 21 volt level, depending upon the actual CR18 breakdown voltage, there will be a level below which CR18, and subsequently Q5, will become nonconductive. When this occurs, the "high" Q5 collector voltage signal applied to Gates Z2E and Z3C results in the UV trip signal at the output of Z3C. The UV trip signal is inhibited at the time 28 VDC power is applied to the SSPC by the power ready (PR) signal to preclude UV trip signals at turn-on.

The UV trip signal results in the setting of the trip lockout (TLO) circuit, so that the SSPC will require resetting in order to return to the ON state even though the 28 VDC supply voltage has returned to normal operating limits. This retentive lockout will preclude load cycling in event of a fluctuating 28 VDC supply voltage.

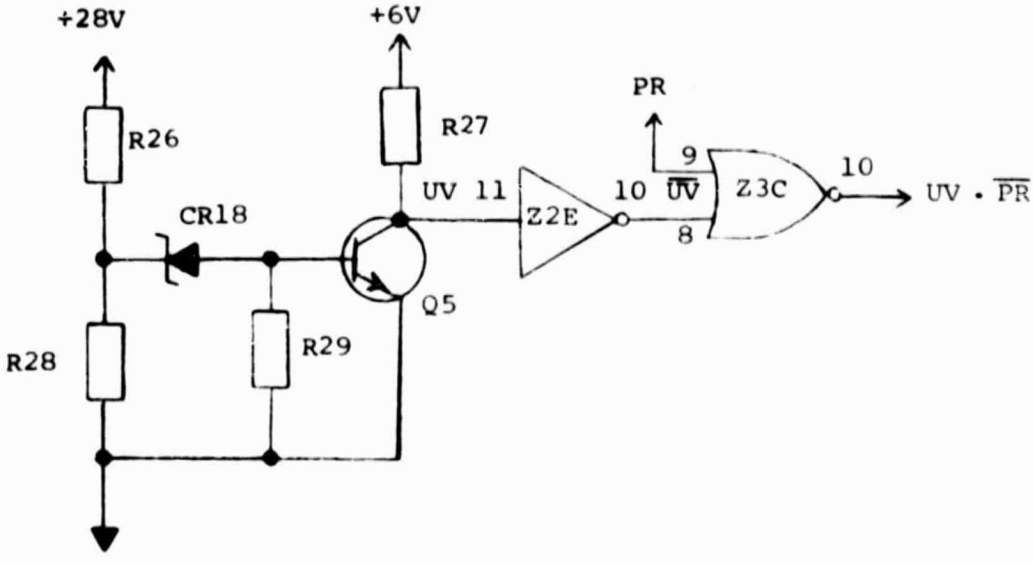


Figure 6-10

28 VDC Undervoltage Protection Circuit

6.4.5 Indication Function Description

6.4.5.1 Status Indication Circuit

The status indication circuit consists of Q6 and associated components. Q6 provides a clamping ground path for a 28 VDC/40 ma load connected to the status indicator terminal. Whenever the TLO circuit is energized, as occurs when the SSPC has been tripped off either by an OC or 28 VDC UV condition, a gate drive signal is applied to Q6 via R30, causing Q6 to be conductive, allowing current to flow in the load connected externally to the SSPC at the status indication terminal. Reverse voltage protection for Q6 is provided by CR19.

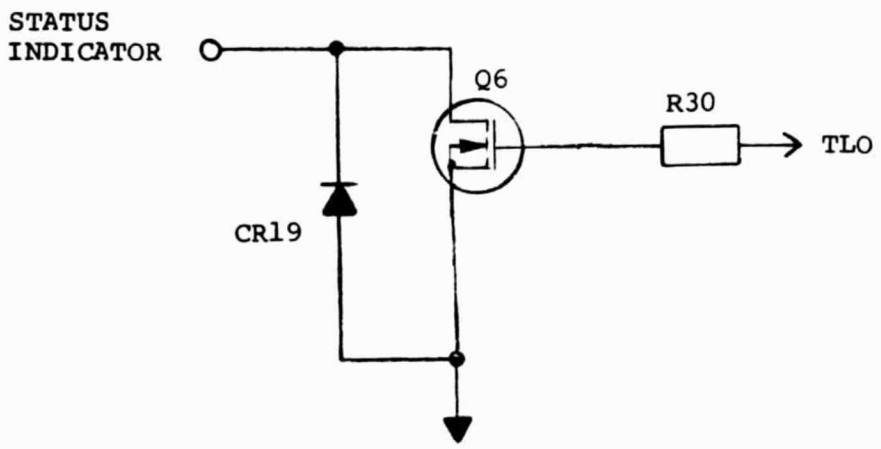


Figure 6-11

Status Indication Circuit

SECTION VII

BREADBOARD TEST AND EVALUATION (TASK VI)

7.1 Task Objectives

a. Provide a test plan which describes the test circuits, test equipment, and the objectives, number, and types of tests to be performed to demonstrate switchgear performance.

b. Evaluate each breadboard model to determine its technical capability to meet the specifications, identify potential problem areas, and incorporate corrective modifications.

c. Record and compile the data for the particular types and designs selected to be fabricated as Engineering Models.

7.2 Test Plans

A synopsis of the test plans for the HVDC EM/SSCB (Type AVC-41) is shown in Table 7-1 and for the HVDC SSPC (Type AVC-43) in Table 7-2. These plans are intended to provide both development and acceptance test data.

7.3 Performance Data Summary

Breadboard performance data is summarized for the two HVDC switchgear designs in Tables 7-3 and 7-4. Pictorial data was also taken, but is not shown here as it will be for the most part a duplication of that appearing in Section IX of this report.

Table 7-1

Summary of the Test Plan for 80A/200-400 VDC EM/SSCB

B/B and Engineering Models

AVC-41 EM/SSCB

Test	Test Conditions	Limits	Performance		
			RT	-55° C	+71° C
Closing Time	28 VDC Close Signal, IL = 50A	10 msec. Max.			
Tripping Time	28 VDC Trip Signal, IL = 50A	10 msec. Max.			
Switch Voltage Drop	IL = 50A	-		-	-
	IL = 80A	.20 VDC Max.			
	IL = 100A	-		-	-
Power Transistor Temperature Rise	After 2 hours switching 300V/80A load at 2 operations per minute and 3% duty cycle	-		-	-
50A, 80A, 100A Switching Operation	Close and Trip At: 1. VDC = 200V, IL = 50A, 80A 100A 2. VDC = 300V, IL = 80A, 100A 3. VDC = 400V, IL = 80A	Pass/Fail Pass/Fail Pass/Fail		- -	- -
Switch Leakage	After 5 operations (at 1 second rate) of 300V/80A	-			
Preshipping Operational Test	Power Switch	Pass/Fail		-	-
	Auxiliary Contacts	Pass/Fail		-	-
	Visual Inspection	Pass/Fail		-	-

Table 7-2

Summary of the Test Plan for 50A/200-400 VDC SSPC B/B and Engineering Models

Item No.	Tests	Temperature °C	B/B Unit	EM Units
1	Dielectric	25	X	X
2	Static Tests	25	X	X
		-40	X	X
		100	X	X
3	T_{on}, T_{off}, T_{rise}, T_{fall}	25	X	X
		-40	X	X
		100	X	X
4	Trip Characteristics	25	X	X
		-40	X	X
		100	X	X
5	Trip Free	25	X	X
		-40	X	X
		100	X	X
6	Reset Time	25	X	X
		-40	X	X
		100	X	X
7	28 VDC Tests	25	X	X
		-40	X	X
		100	X	X
8	Short Circuit Response	25	X	X
		-40	X	X
		100	X	X
9	Transient Voltage Tests	25	-	X
10	Vacuum Chamber Tests	25	-	X

Table 7-3

Breadboard Test Data

AVC-41 EM/SSCB

Unit Serial No. - Breadboard

Test	Test Conditions	Limits	Performance		
			RT	-55°C	+71°C
Closing Time	28 VDC Close Signal, IL = 50A	10 msec. Max.	7.4 ms.	7.0 ms.	7.5 ms.
Tripping Time	28 VDC Trip Signal, IL = 50A	10 msec. Max.	4.0 ms.	5.2 ms.	4.4 ms.
Switch Voltage Drop	IL = 50A	-	-	-	-
	IL = 80A	.20 VDC Max.	.130	.107	.144
	IL = 100A	-	-	-	-
Power Transistor Temperature Rise	After 2 hours switching 300V/80A load at 2 operations per minute and 3% duty cycle	-	2°C	-	-
50A, 80A, 100A Switching Operation	Close and Trip At:				
	1. VDC = 200V, IL = 50A, 80A 100A	Pass/Fail	Pass	-	-
	2. VDC = 300V, IL = 80A, 100A	Pass/Fail	Pass	Pass	Pass
	3. VDC = 400V, IL = 80A	Pass/Fail	Pass	-	-
Switch Leakage	After 5 operations (at 1 second rate) of 300V/80A	-	1.9 ma.	2.0 ma.	2.05 ma.
Preshipping Operational Test	Power Switch	Pass/Fail	Pass	-	-
	Auxiliary Contacts	Pass/Fail	Pass	-	-
	Visual Inspection	Pass/Fail	Pass	-	-

Table 7-4

AVC-43 SSPC Breadboard Performance Summary

Parameter	Special Limit (D-774149)	Measured Values (-40°C to +100°C)
Power Switch Leakage	5.0 ma Max.	.008-.710 ma
Power Switch Voltage Drop	1.90 VDC Max. @ 50A	1.78 VDC
SSPC Power Dissipation	100W Max. "ON" 5.0W Max. "OFF" 5.0W Max. "TRIPPED"	73.7-92.4W .78-1.06W 1.23-1.60W
SSPC Efficiency	99.0% Min.	99.1-99.6%
Overshoot	3,000% Max. Amplitude 10 µsec. Max. Time	0 0
SSPC Response Times	.01-10 msec. Turn-On 10-500 µsec. Rise Time .01-10 msec. Turn-Off 10-1,000 µsec. Fall Time	6.5-8.8 msec. 80-100 µsec. 6.6-9.5 msec. 85-370 µsec.
OC Tripping Times	55-70A Min. PU .25 Sec. Min. @ 65A .10 Sec. Min. @ 70A .02-1.8 Sec. @ 80A 0-0.3 Sec. @ 90A 0-0.06 Sec. @ 100A	62.8-69.0A 2.2 Sec. Min. .325 Sec. Min. .035-.046 Sec. .0004-.025 Sec. ------
28 VDC Input Current	150 ma Max.	120 ma
28 VDC UV Protection	15-21 VDC Min. PU 5-15 msec. Time Delay	17.4-17.8 VDC 8-11 msec.
Control Circuit	4.0 VDC Max. Turn-On 2.0 VDC Min. Turn-Off	2.60-3.27 VDC 2.41-2.77 VDC
Time to Reset	3-15 msec.	5-8 msec.
Status Indication	.5 VDC Sat. Volt @ 40 ma (Tripped) 10 a Leakage Max. @ 30 VDC (OFF/ON)	.110-.119 VDC (10 ma) 0

SECTION VIII

ENGINEERING MODELS, DESIGN, AND FABRICATION (TASK VI)

8.1 Task Objectives

a. Make detailed designs and fabricate four (total) Engineering Models of the selected types of switchgear.

b. These models shall be capable of vacuum chamber operations at pressures in the range of 10^{-5} to 10^{-7} torr.

8.2 EM/SSCB Packaging Design

The packaged Engineering Model design is shown in the Figure 8-1, Outline Drawing. With NASA's approval, this unit was not fully designed for operation in the vacuum. Figure 8-2 depicts the construction details of the design.

The electro-mechanical portion consists of the high performance Westinghouse Aircraft Circuit Breaker to which was added a breaker cross-section sized printed circuit board containing the solid state commutation circuit components. The case was then modified in height to incorporate the added components and to provide a slightly "stretched" version of the original CB design. Three units were made of this design: one Westinghouse development unit, plus two Engineering Models - one for NASA and one for the Boeing Company's (Seattle, Washington) developmental evaluation.

1. DIMENSIONS IN INCHES (MM)

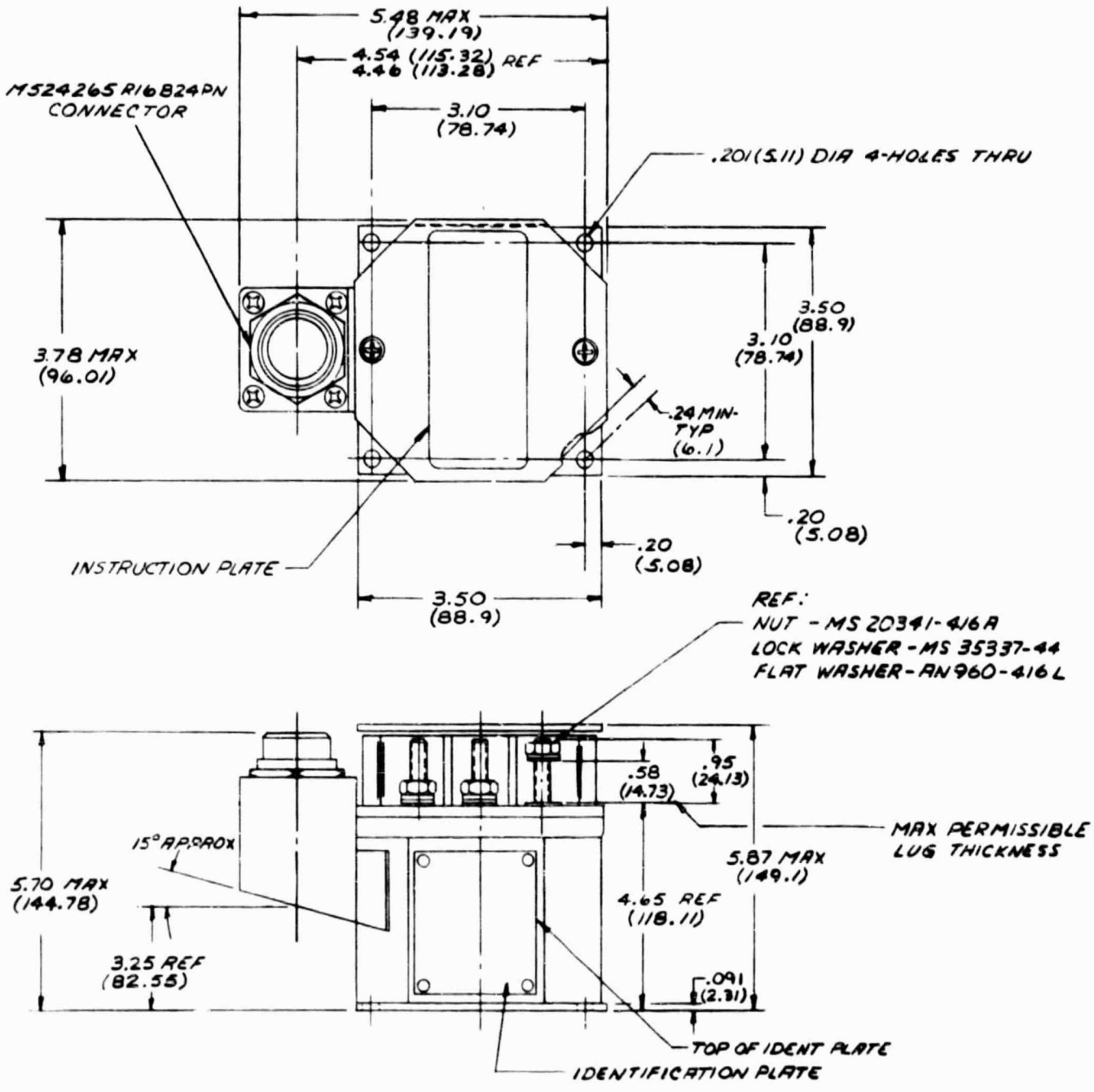


Figure 8-1

80A/400 VDC EM/SSCB Outline Drawing (Type AVC-41)

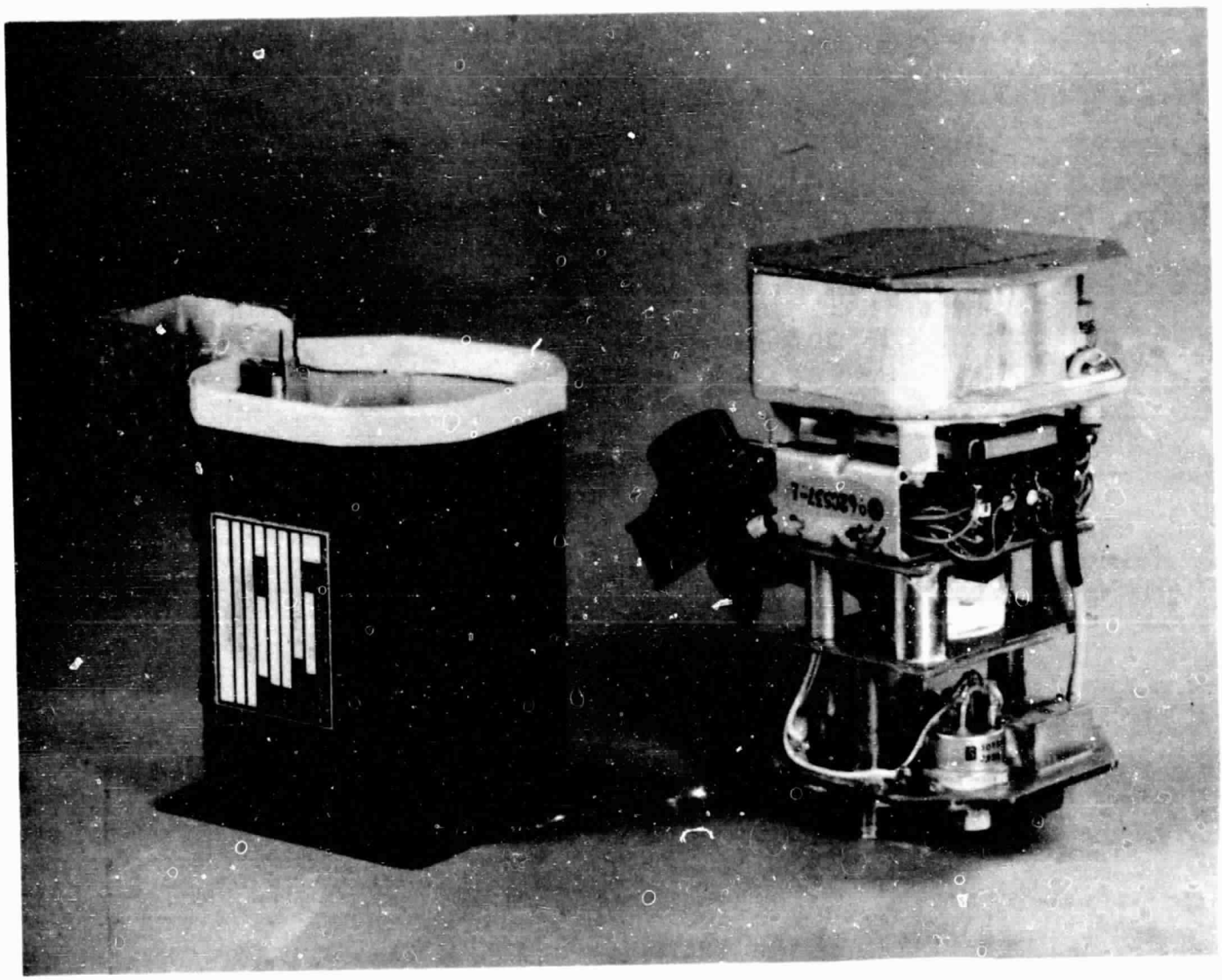


Figure 8-2

Type AVC-41 80A/400 VDC EM/SSCB Assembly Picture

8.3 HVDC SSPC Packaging Design

Figure 8-3, Outline/Installation Drawing, depicts the 400V/50A SSPC Engineering Models. The units are designed for cold plate mounting to provide cooling by conduction through the base to the mounting surface; this is a must for vacuum operation. Additional convection cooling for non-vacuum operation is provided by the perforated cover.

Figure 8-4 depicts external and internal construction details. The low level electronic components are mounted on two printed circuit boards. The smaller dissipation parts are mounted on an epoxy-coated bracket while the power switch transistors are mounted on a copper heat sink. Two circular connectors are utilized; the smaller one for control circuits, the larger one for HVDC power. The copper channel heat sink was modified as follows during the evaluation tests:

a. originally it was .090 aluminum and was changed to .125 copper to reduce the thermal drop; and

b. the transistor mounting surface was finished to 16 microinch with .00025 in./in. flatness to enhance heat transfer in a vacuum environment.

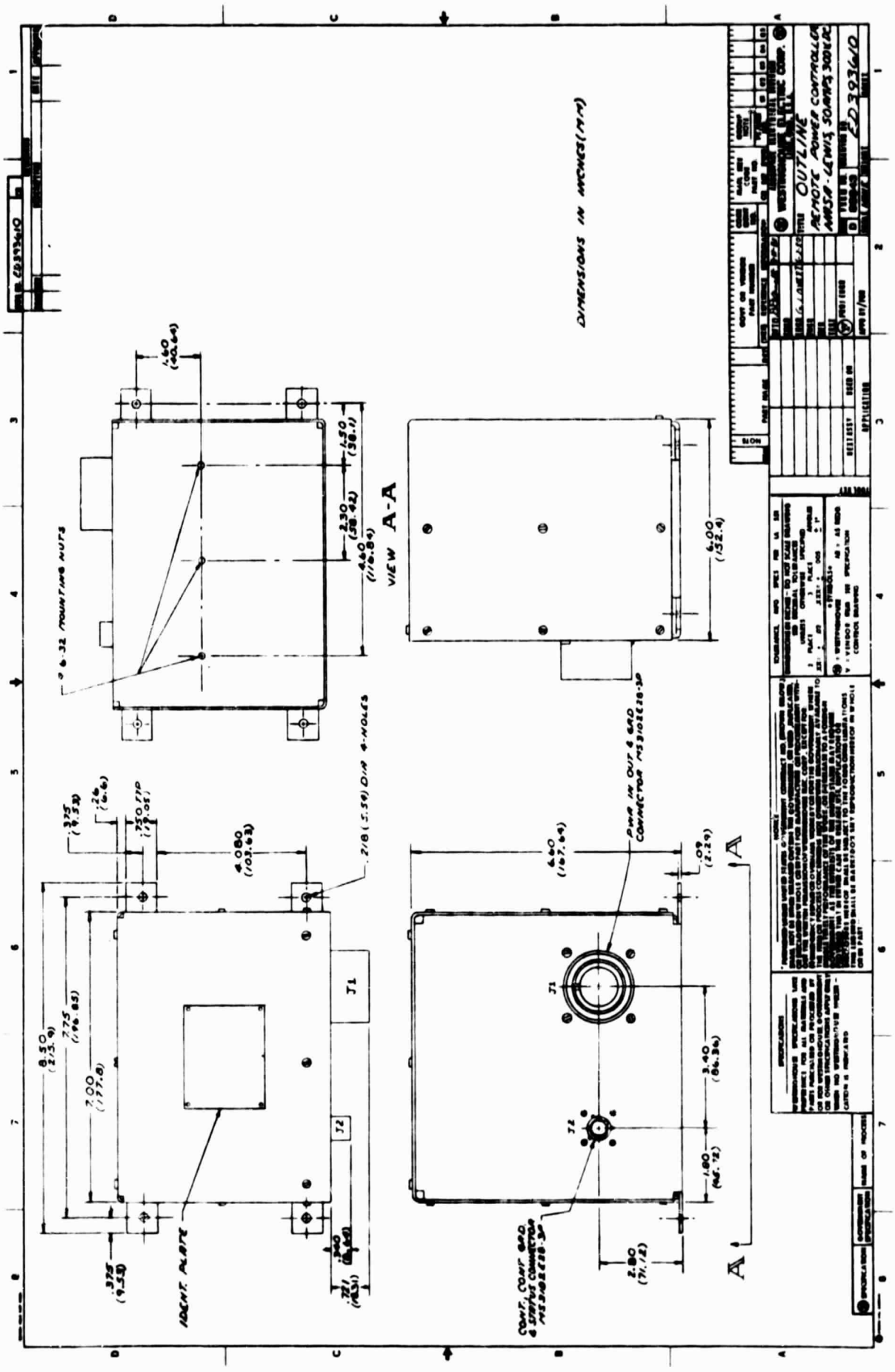


Figure 8-3

Type AVC-43 SSPC Outline Drawing

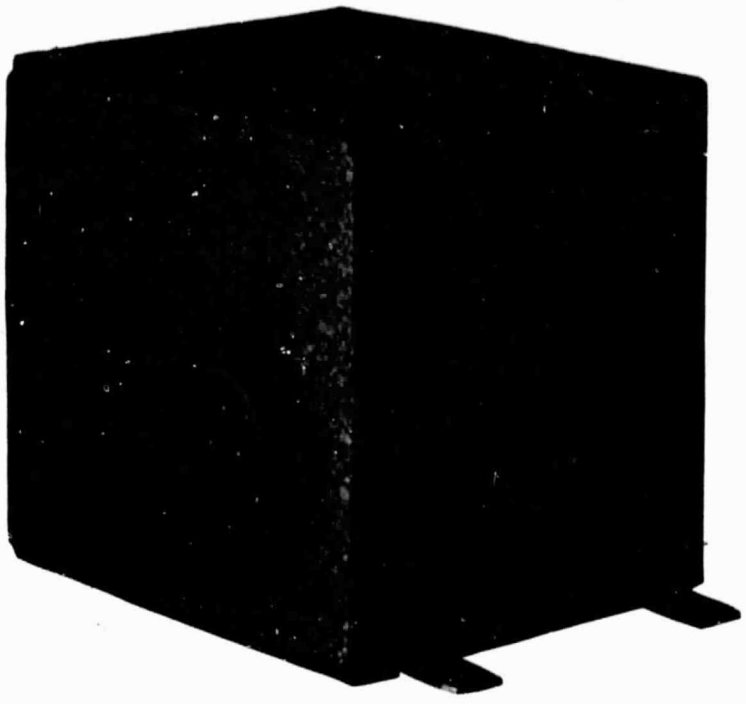


Figure 8-4A

Type AVC-43 SSCB

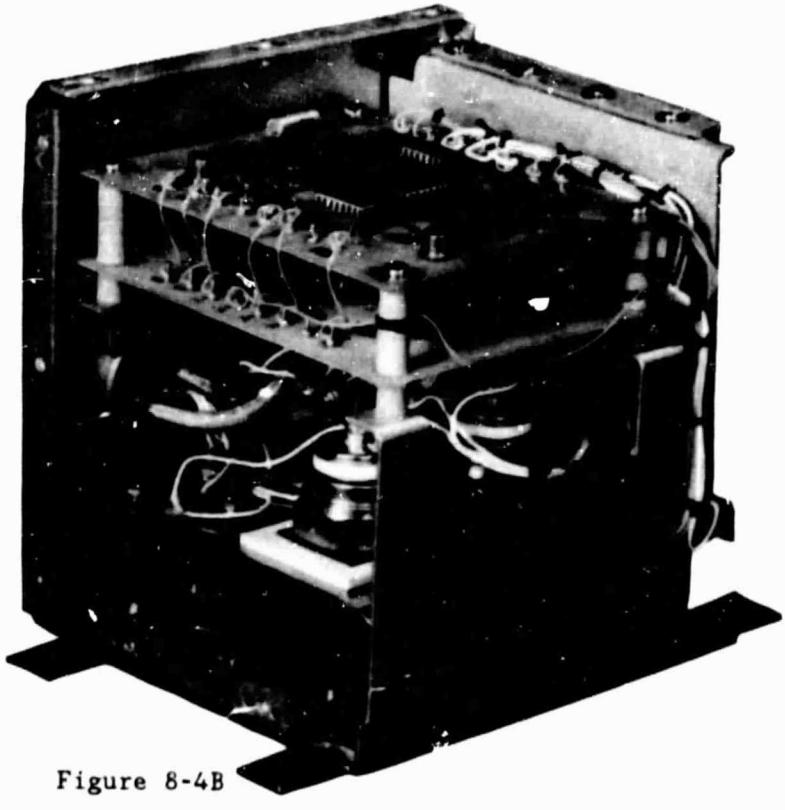


Figure 8-4B

Type AVC-43 SSCB Assembly View

SECTION IX

TEST AND EVALUATION (TASK VII)

9.1 Task Objectives

The goals of this task were to:

a. evaluate unit performance and capabilities;

b. verify compliance to specification requirements; and

c. compile and analyze test data.

9.2 EM/SSCB Evaluations

Included in the following test data are significant parameter measurements and oscilloscope pictures depicting dynamic operating performance. Tables 9-1 and 9-2 are a compilation of measurements for the two units per the Test Plan of Section VII. Figures 9-1 through 9-4 show operations for loads of 50A, 80A, and 100A; supply voltages of 200, 300, and 400 VDC; and temperatures of -55°C, RT, and +71°C. Noteworthy results are the low switch drops of .057 volts maximum and the low internal temperature rise under load switching operation.

Table 9-1

Performance Test Data, Unit No. 1

AVC-41 EM/SSCB

Test	Test Conditions	Limits	Performance		
			RT	-55°C	+71°C
Closing Time	28 VDC Close Signal, IL = 50A	10 msec. Max.	6.3 ms.	6.3 ms.	6.8 ms.
Tripping Time	28 VDC Trip Signal, IL = 50A	10 msec. Max.	5.6 ms.	6.3 ms.	6.9 ms.
Switch Voltage Drop	IL = 50A	-	.032V	-	-
	IL = 80A	.20 VDC Max.	.043V	.057V	.049V
	IL = 100A	-	.057V	-	-
Power Transistor Temperature Rise	After 2 hours switching 300V/80A load at 2 operations per minute and 3% duty cycle	-	2°C Rise Above Ambient	-	-
50A, 80A, 100A Switching Operation	Close and Trip At:				
	1. VDC = 200V, IL = 50A, 80A 100A	Pass/Fail	Pass	-	-
	2. VDC = 300V, IL = 80A, 100A	Pass/Fail	Pass	Pass	Pass
	3. VDC = 400V, IL = 80A	Pass/Fail	Pass	-	-
Switch Leakage	After 5 operations (at 1 second rate) of 300V/80A	-	2.0 ma	1.9 ma	2.0 ma
Preshipping Operational Test	Power Switch	Pass/Fail	Pass	-	-
	Auxiliary Contacts	Pass/Fail	Pass	-	-
	Visual Inspection	Pass/Fail	Pass	-	-

Table 9-2

Performance Test Data, Unit No. 2

AVC-41 EM/SSCB

Test	Test Conditions	Limits	Performance		
			RT	-55°C	+71°C
Closing Time	28 VDC Close Signal, IL = 50A	10 msec. Max.	6.4 ms.	6.9 ms.	7.0 ms.
Tripping Time	28 VDC Trip Signal, IL = 50A	10 msec. Max.	4.8 ms.	4.7 ms.	5.0 ms.
Switch Voltage Drop	IL = 50A	-	.024V	-	-
	IL = 80A	.20 VDC Max.	.044V	.055V	.049V
	IL = 100A	-	.056V	-	-
Power Transistor Temperature Rise	After 2 hours switching 300V/80A load at 2 operations per minute and 3% duty cycle	-	2°C Rise Above Ambient	-	-
50A, 80A, 100A Switching Operation	Close and Trip At:				
	1. VDC = 200V, IL = 50A, 80A 100A	Pass/Fail	Pass	-	-
	2. VDC = 300V, IL = 80A, 100A	Pass/Fail	Pass	Pass	Pass
	3. VDC = 400V, IL = 80A	Pass/Fail	Pass	-	-
Switch Leakage	After 5 operations (at 1 second rate) of 300V/80A	-	2.0 ma	1.9 ma	2.0 ma
Preshipping Operational Test	Power Switch	Pass/Fail	Pass	-	-
	Auxiliary Contacts	Pass/Fail	Pass	-	-
	Visual Inspection	Pass/Fail	Pass	-	-

Figure 9-1

AVC-41 EM/SSCB

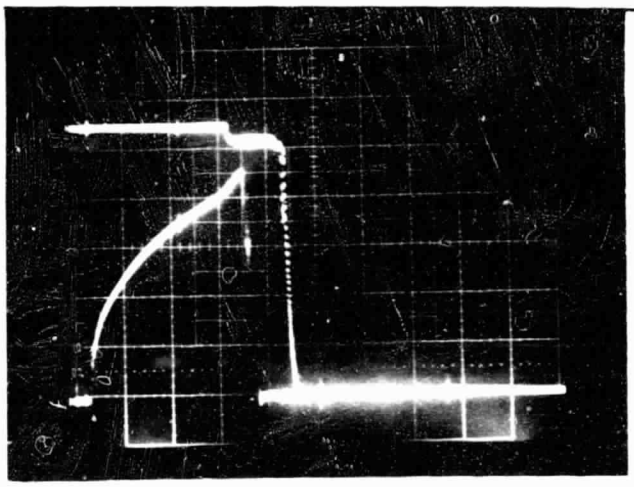
Close and Trip Coil Current Waveforms

300V/80A DC Load

Load Voltage Vs. Trip and Close Currents

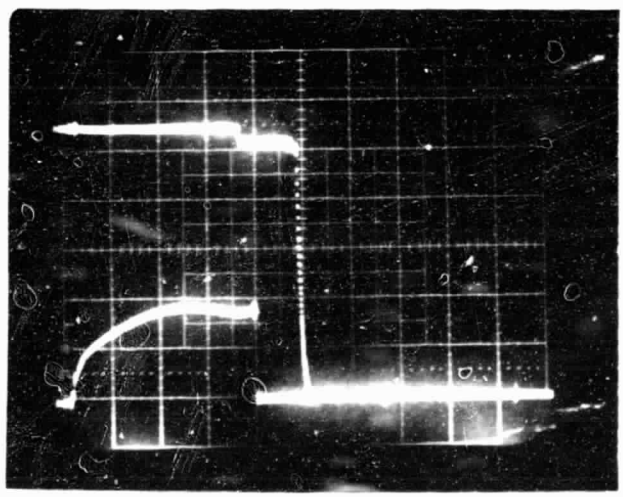
Top: V_{load} = 50V/div. t = 1 msec./div.

Bottom: I_{trip} = .4A/div. (30 VDC)



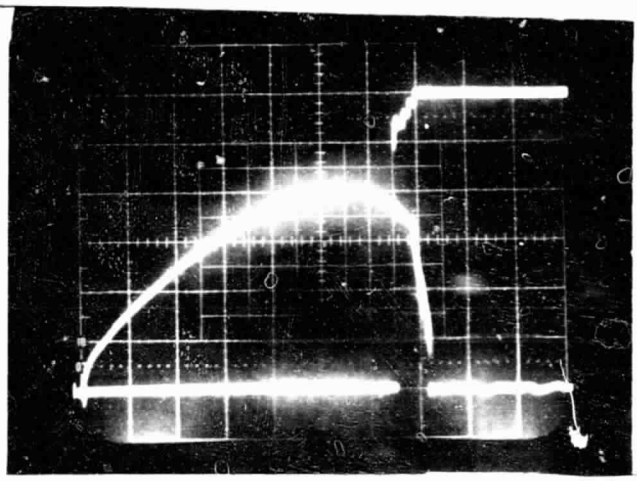
V_{trip} = 15 VDC t = 1 msec.

I_{trip} = .4A/div.



Top: V_{load} = 50 div.. t = 1 msec./div.

Bottom: I_{close} = 1A/div. (30 VDC)



V_{close} = 15 VDC t = 2 msec./div.

I_{close} = .4A/div.

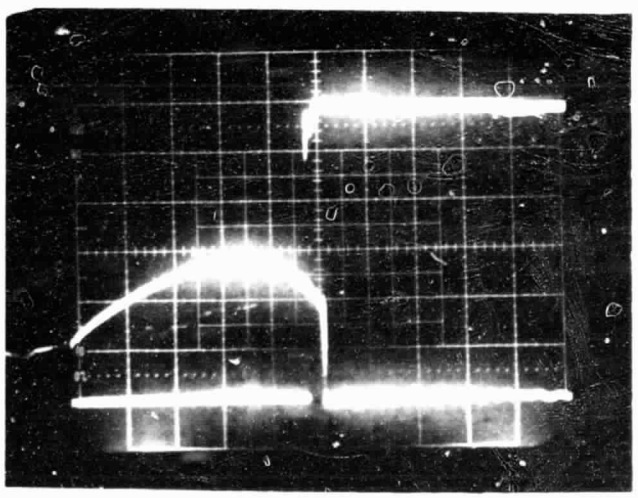


Figure 9-2

AVC-41 EM/SSCB

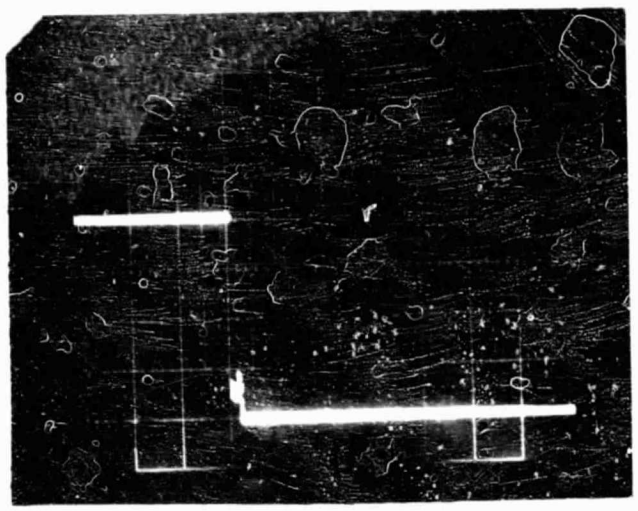
200 VDC Operation

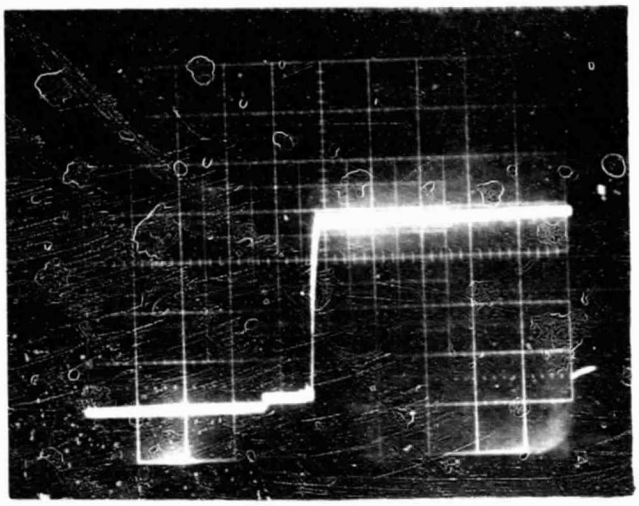
Switch Voltage Waveforms

Close and Trip Signals = 30 VDC

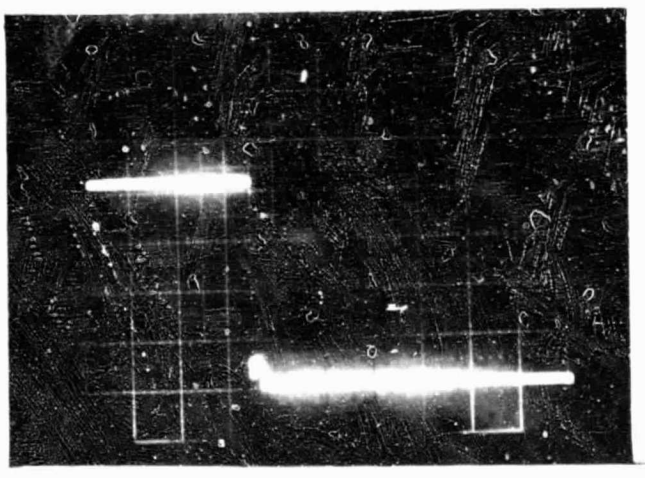
Close: 2 msec./div. Trip: 1 msec./div.

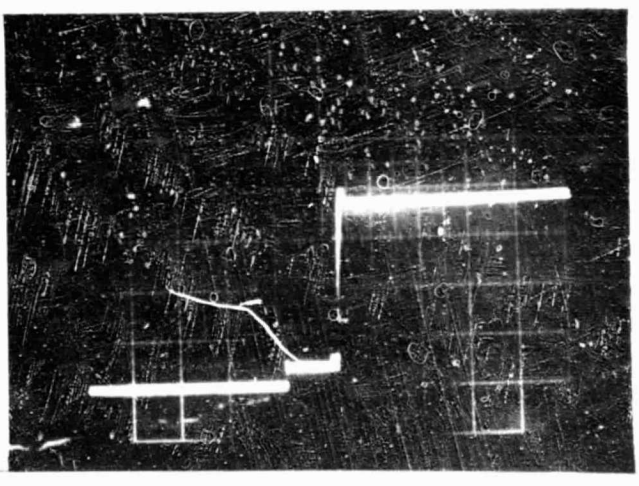
200 VDC/50A Operation





200 VDC/100A Operation





For All Pictures: V_{switch} = 50V/div.

Figure 9-3

AVC-41 EM/SSCB

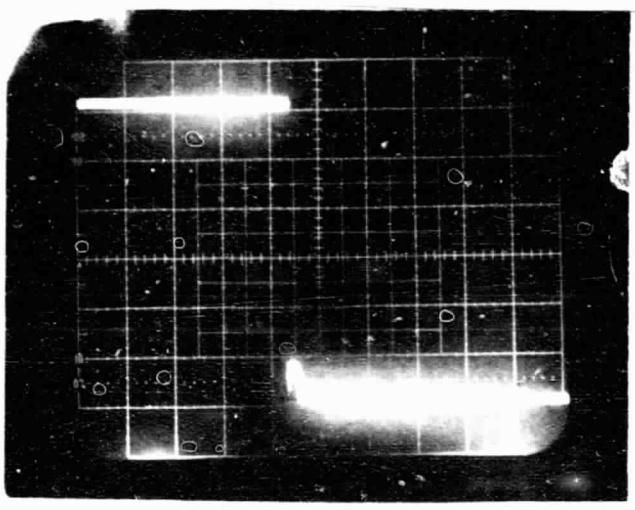
300 VDC and 400 VDC Operation

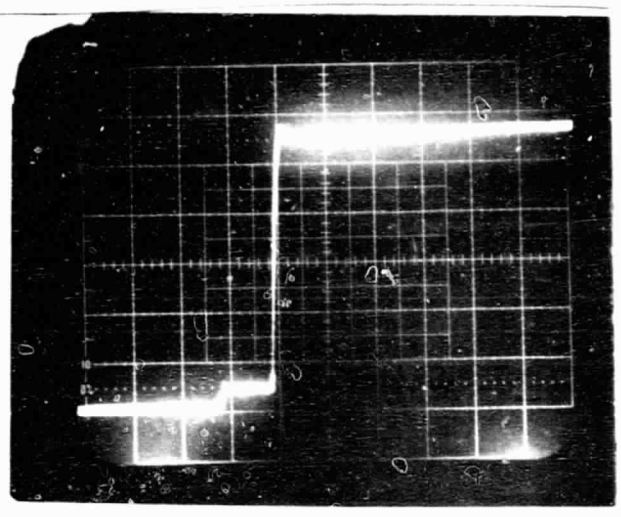
Switch Voltage Waveforms

Close and Trip Signals = 30 VDC

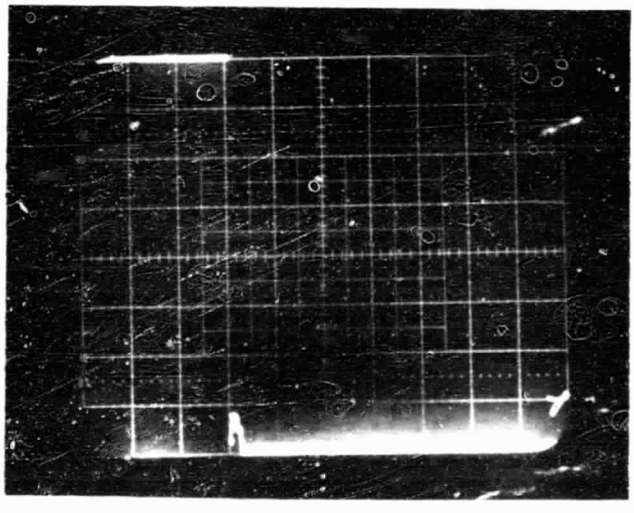
Close: 2 msec./div. Trip: 1 msec./div.

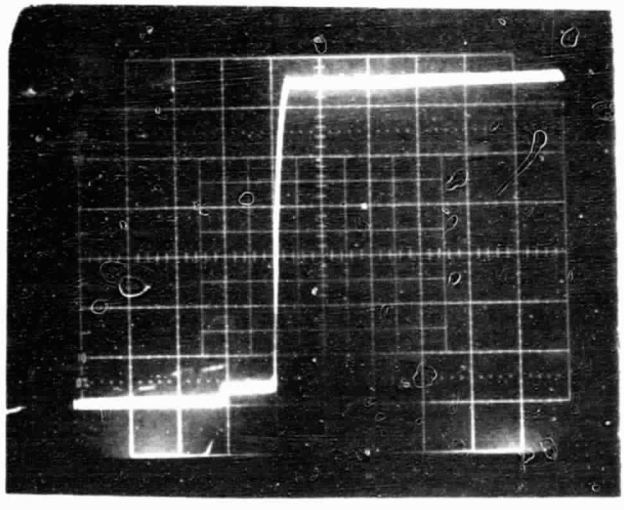
300 VDC/100A Operation





400 VDC/80A Operation





For All Pictures: V_{switch} = 50V/div.

Figure 9-4

AVC-41 EM/SSCB

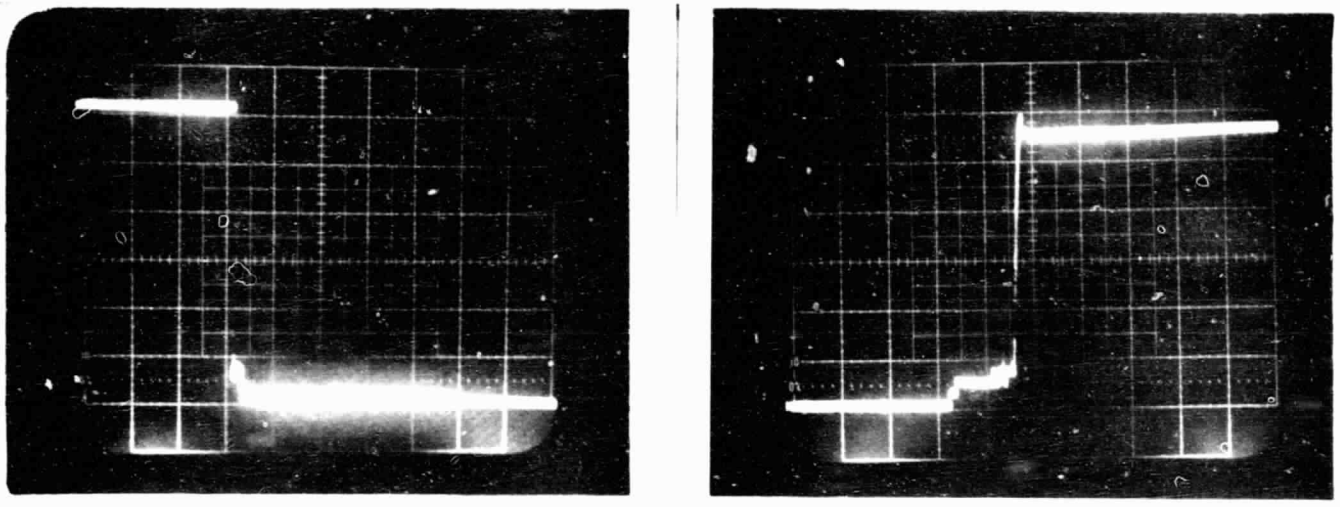
-55°C and +71°C Performance

300 VDC/80A Operation

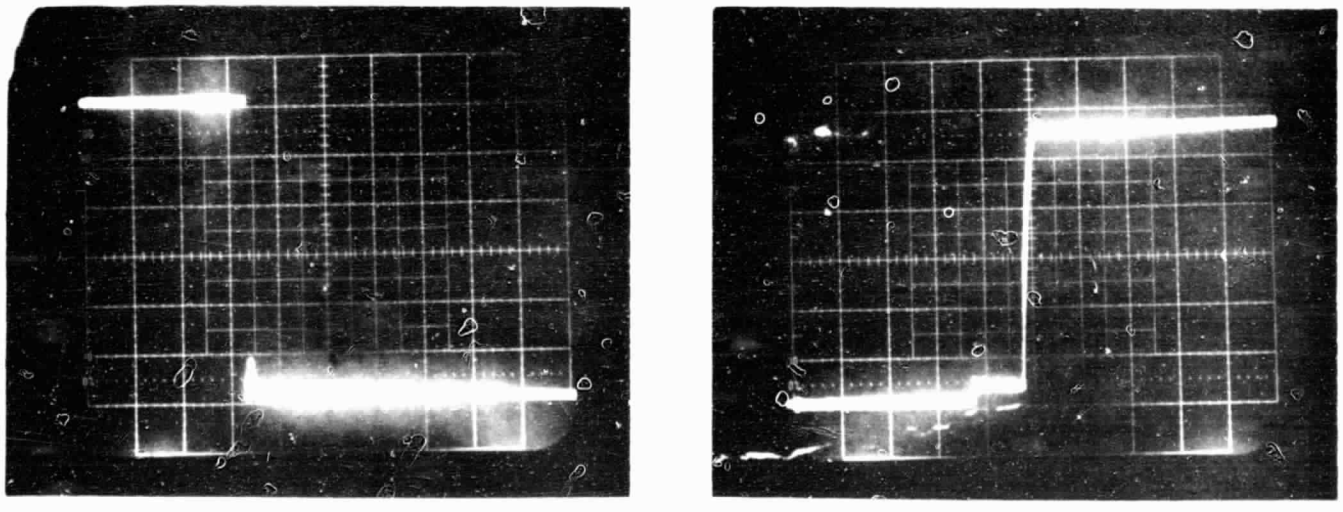
Close and Trip Signals = 30 VDC

Close: 2 msec./div. Trip: 1 msec./div.

-55°C Ambient



+71°C Ambient



For All Pictures: V_{switch} = 50V/div.

9.3 HVDC SSPC Evaluation

Table 9-3 is a summary of significant test data for the three Engineering Model HVDC SSPCs. Figures 9-5 through 9-7 are plots of parametric data. Load switching oscilloscope pictures are shown in Figure 9-8, while overload and short circuit performances are shown in Figures 9-9 and 9-10. The 1000V spike transient test response is shown in Figure 9-11, and turn-on into the critical value of load capacitance for this design, 10 μF, which just causes SSPC trip-off at turn-on. The amount of resistive load in parallel from 5A to 50A, has little effect on whether SSPC will or will not trip off, although the trip-off time varies slightly from 90 μseconds at 5A load to 75 μseconds at 50A preload.

Table 9-3

Summary of Significant Test Data

Item	Temperature °C	Serial #1, 2, & 3	Units
Dielectric Test	25	OK	---
"ON" Dissipation	-40 to +100	66.4 to 90.6	Watts
"ON" Efficiency	-40 to +100	99.4 to 99.6	%
"OFF" Dissipation	-40 to +100	.70 to 1.13	Watts
Turn-On Time	-40 to +100	5.0 to 7.0	Milliseconds
Rise Time	-40 to +100	140 to 160	Microseconds
Turn-Off Time	-40 to +100	5.4 to 8.5	Milliseconds
Fall Time	-40 to +100	80 to 370	Microseconds
Short Circuit Peak Let-Through Current	-40 to +100	92 to 180	Amperes
+1000V Spike Test	25	OK	---
-1000V Spike Test	25	OK	
Maximum Load Capacitance	25	10	Microfarads
Overcurrent	-40 to +100	See Figure 9-5	---

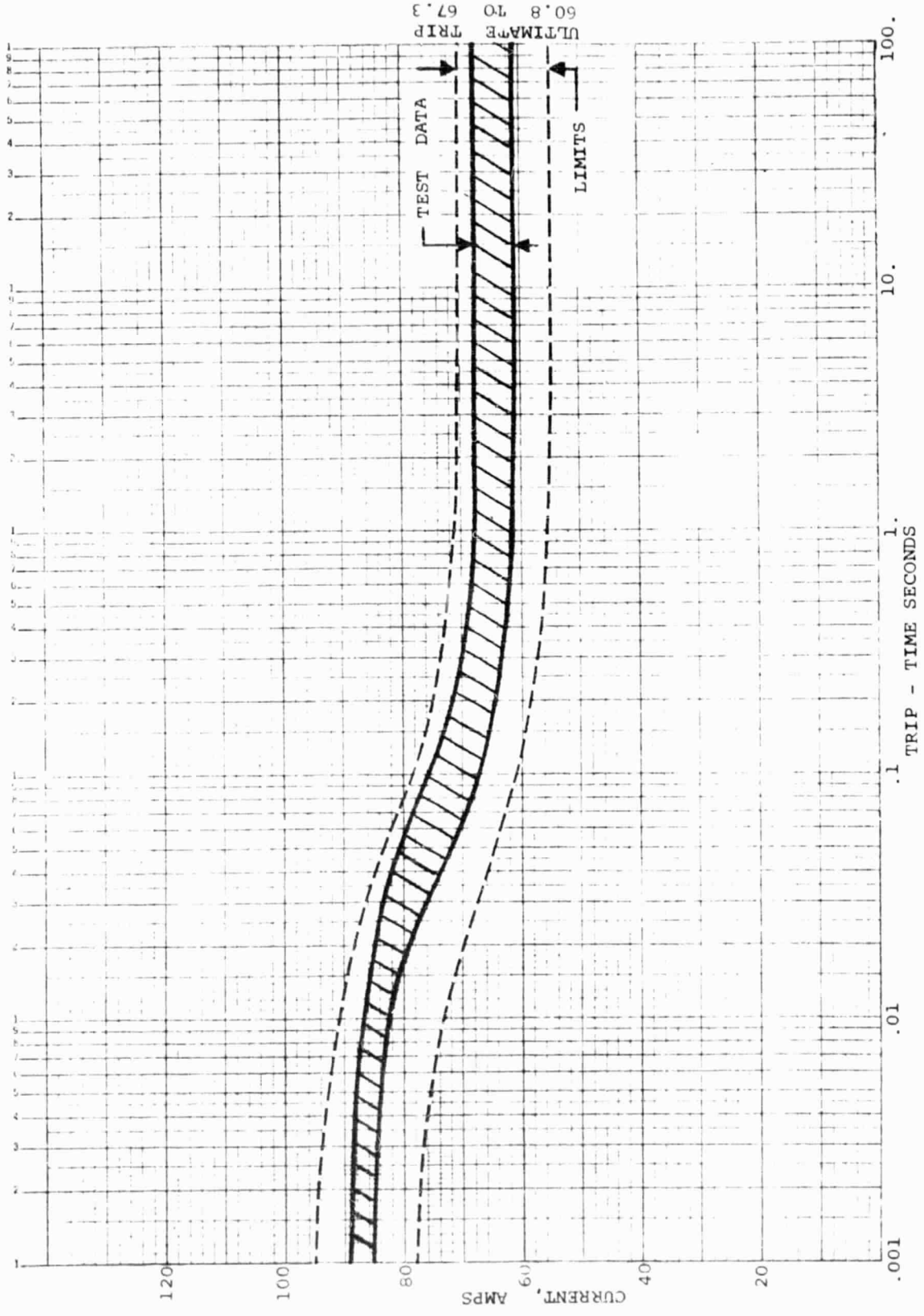


Figure 9-5

Overcurrent Trip Time Characteristics

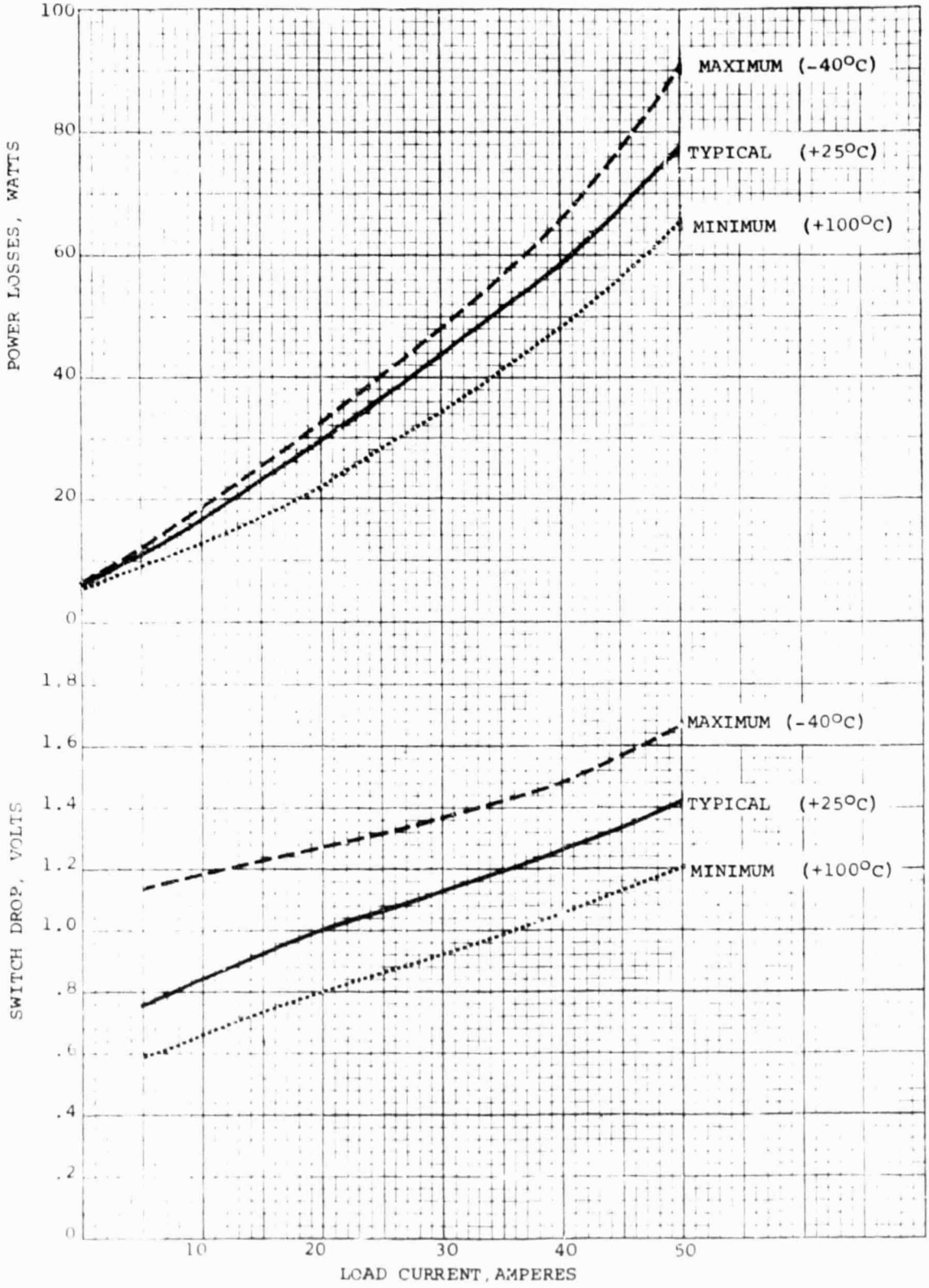


Figure 9-6

SSPC Power Loss and Switch Drop Vs. Load Current

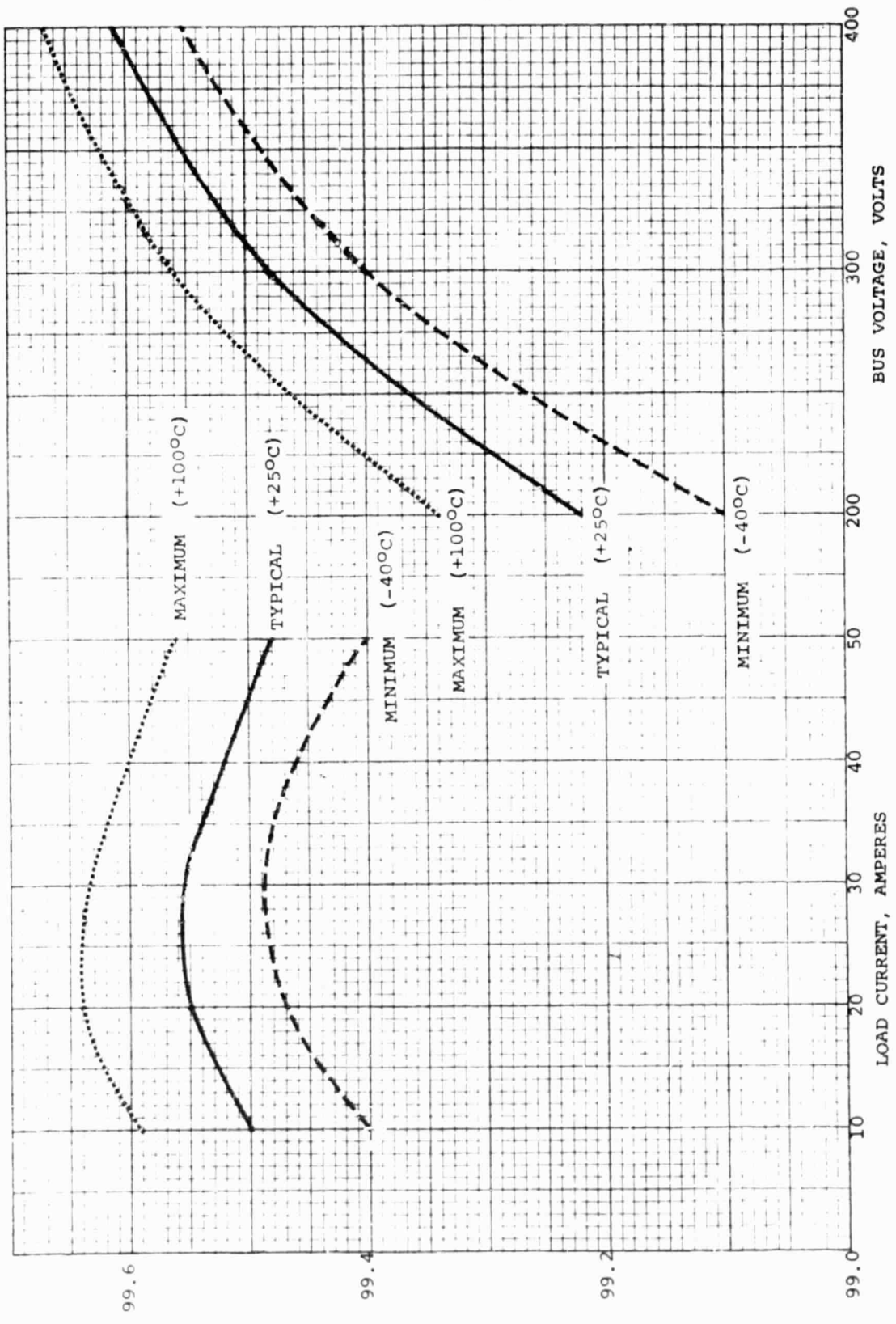


Figure 9-7

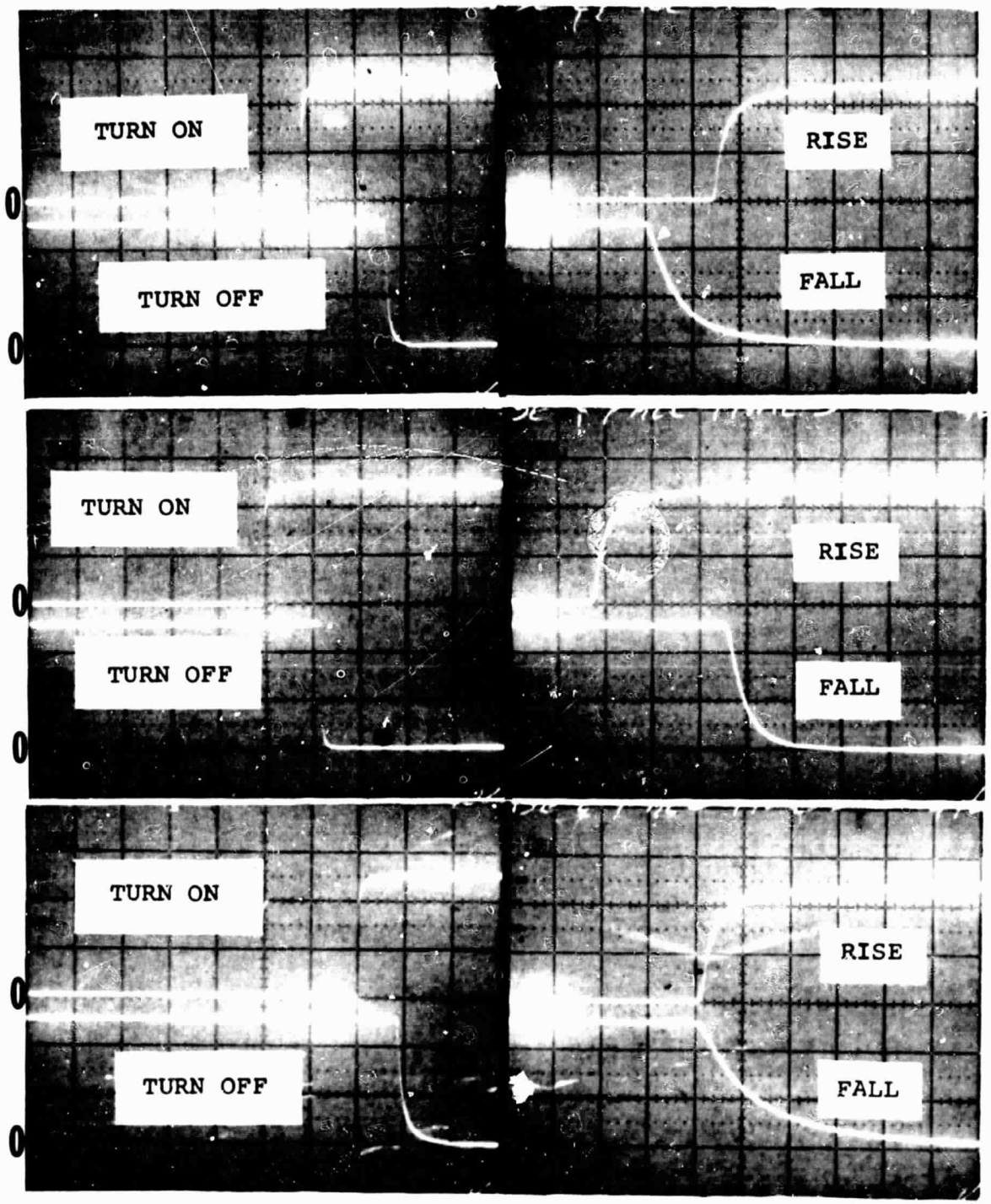
SSPC Efficiency Vs. Load Current and Supply Voltage

Figure 9-8

Turn-On/Turn-Off, Rise & Fall Times

Load Current 20A/Div. Vs. Temperature

Time 1 ms./div. Time 100 µsec./div.



0066R

Figure 9-9

Overcurrent Trip Times Vs. Temperature

Load Current 20A/Div.

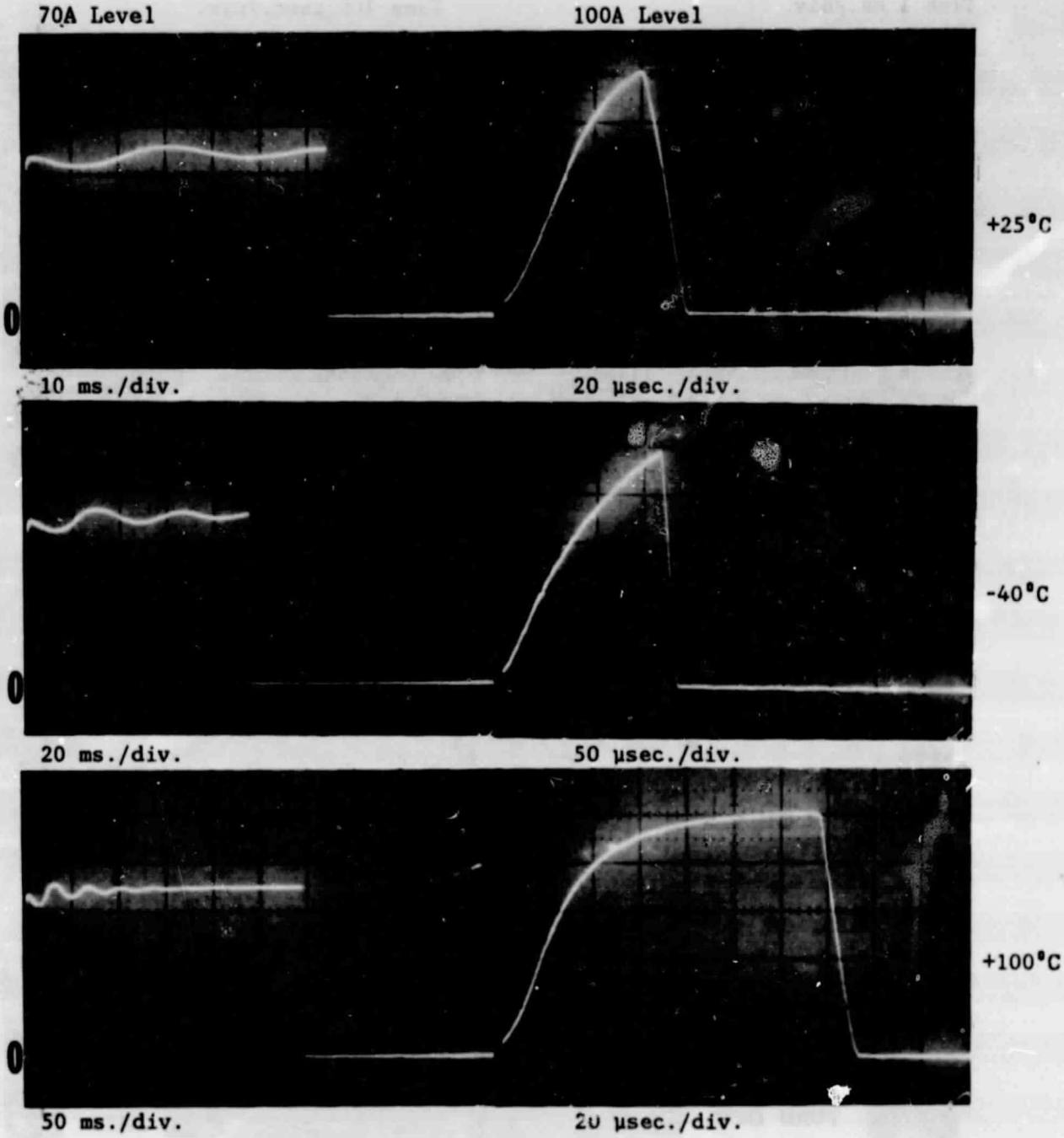


Figure 9-10

Short Circuit Trip Times Vs. Temperature

Load Current 40A/Div.

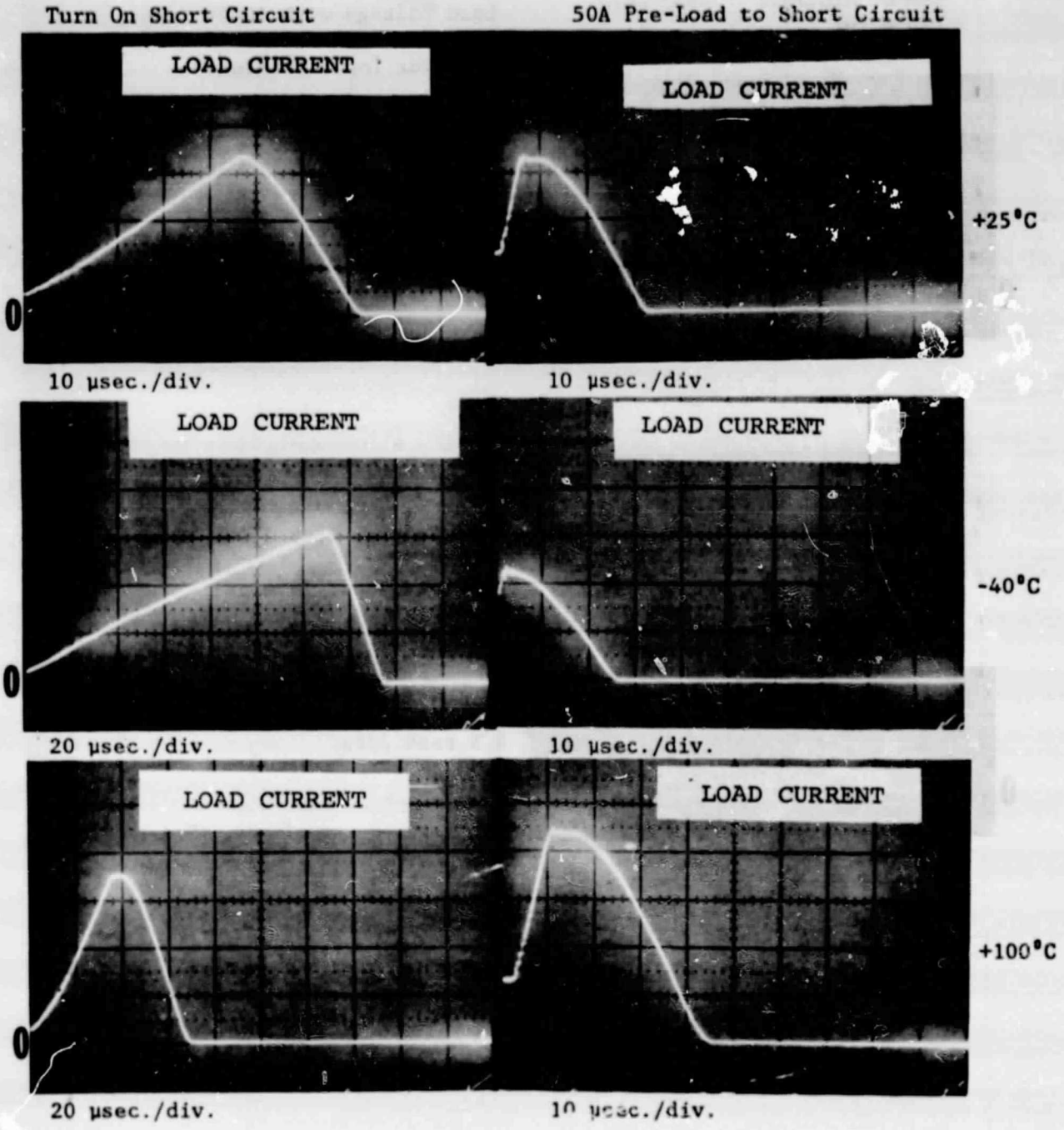
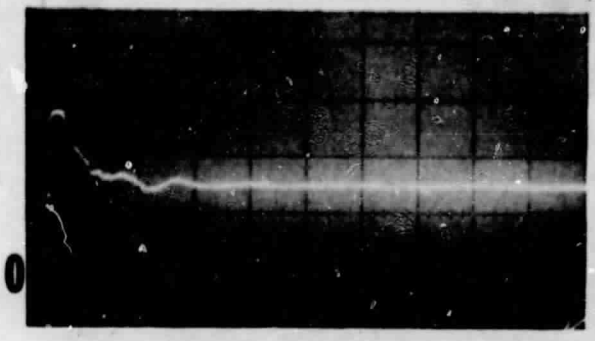


Figure 9-11

Transient Voltage Tests

LOAD VOLTAGE TERMINAL
SSCB ON



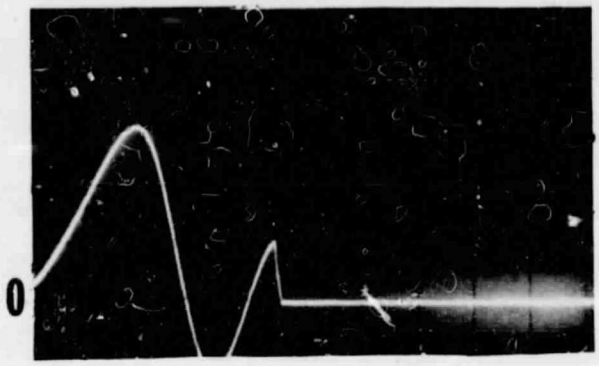
Load Voltage with 1000V Transient
at Power Input Terminal
SSCB ON
200V/div.
0.5 μsec./div.

LOAD VOLTAGE TERMINAL
SSCB OFF

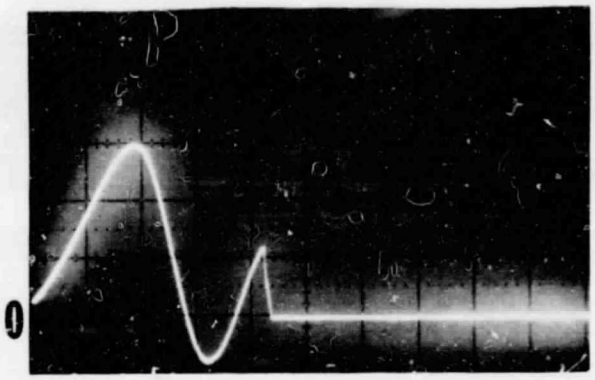
Load Voltage with 1000V Transient
at Power Input Terminal
SSCB OFF
200V/div.
0.5 μsec./div.

Figure 9-12

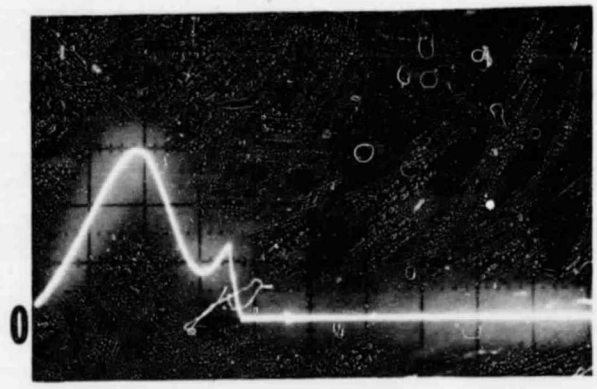
Capacitive Load Tests



Load Current Turn-On Into 10 µF
and 5A Load
40A/div.
20 µsec./div.



Load Current Turn-On Into 10 µF
and 25A Load
40A/div.
20 µsec./div.



Load Current Turn-On Into 10 µF
and 50A Load
40A/div.
20 µsec./div.

9.4 HVDC SSPC Vacuum Chamber Test

9.4.1 Test Objectives

The purpose of this evaluation is to verify and measure SSPC performance under a vacuum condition. The following tests will be performed on one EM unit at a vacuum of 10^{-4} to 10^{-6} torr and at 25 $\pm$ 5°C ambient.

a. Dielectric test between all terminals to case and power terminals to control terminals.

b. Take oscilloscope pictures of the SSPC switch voltage for turn-on and turn-off with 300 VDC/50A load.

c. Measure and record power transistor heat sink, case, and mounting plate temperatures (stabilized values) with 50A load condition.

d. Measure the SSPC switch drop, load current, 28 VDC supply voltage, and current.

9.4.2 Test Summary

The test set-up is shown in Figure 9-13, and significant results of this test are as follows:

Test Pressure	10^{-5} torr (approx. 80 miles altitude)
Dielectric Test	Leakage @ 1 KVDC is less than .23 μa.
θ (D60T - Heat Sink)	.11°C/W
θ (Heat Sink - Base)	.29°C/W
θ (Base - Mounting Plate)	.55°C/W
θTOT (D60T - Mounting Plate)	.95°C/W
PDISS @ 300 VDC/50A Load	114W
Efficiency @ 300 VDC/50A Load	99.2%
Max. Cold Plate Oper. Temp.	10°C (50°F)*

The Thermal Data Plot, Figure 9-14, shows the thermal drop profile which represents virtually stabilized values. Figures 9-15 and 9-16 show the NICOLET Storage Displays of load switching; room ambient and vacuum operation are essentially the same.

*Based on 100W maximum dissipation and D60T transistor maximum case temperature of 105°C using AS-4613, Class A Reliability Criteria.

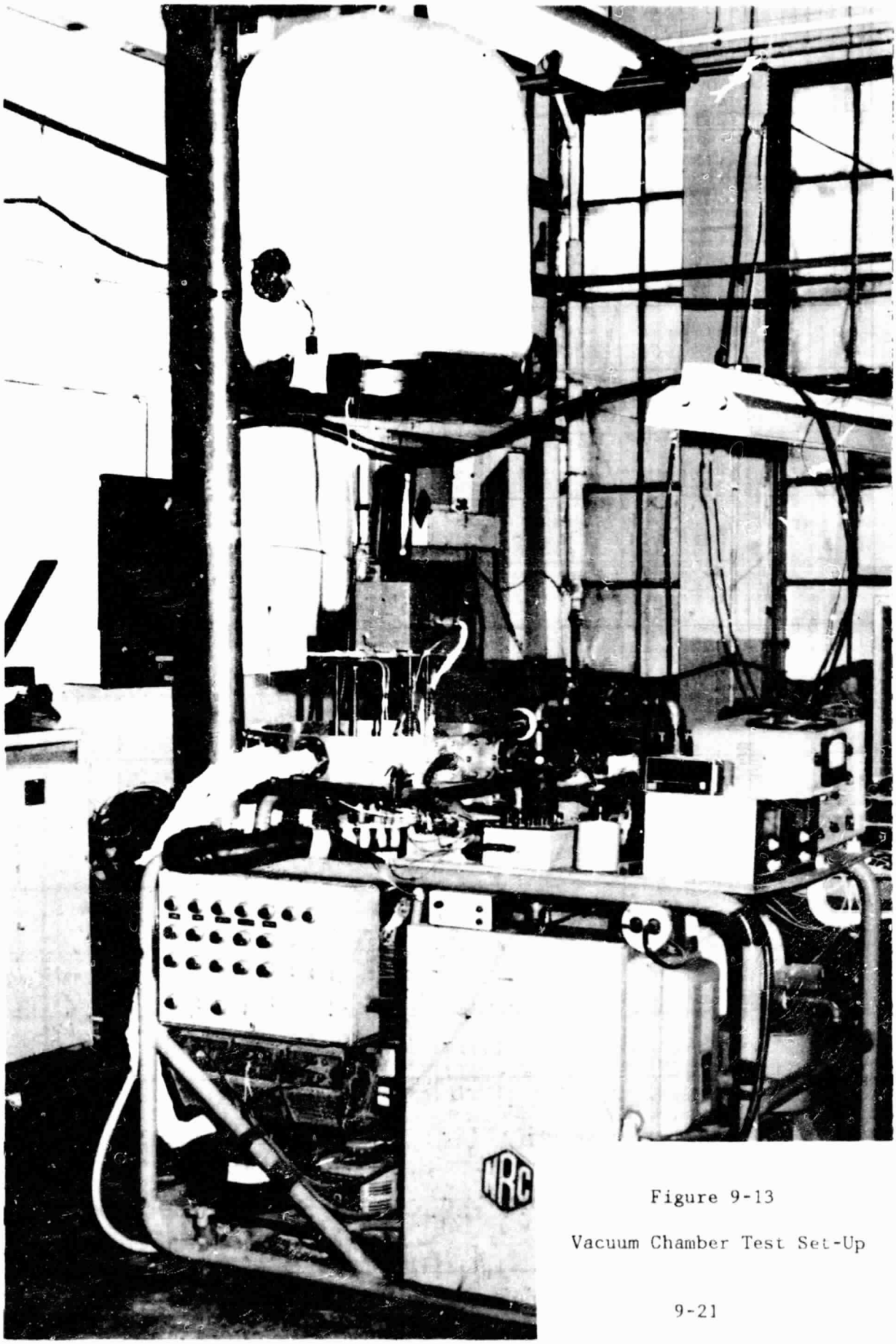


Figure 9-13

Vacuum Chamber Test Set-Up

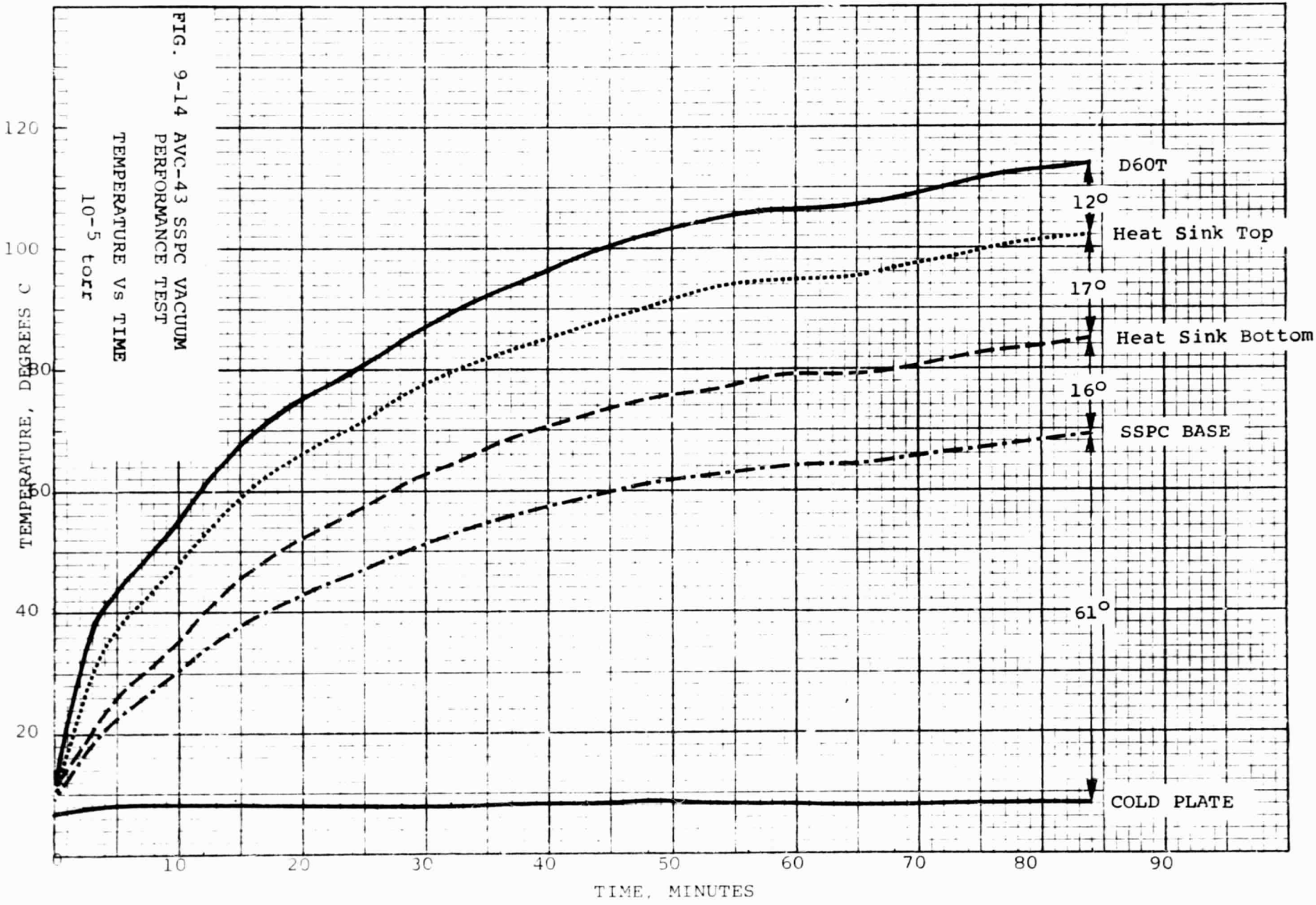


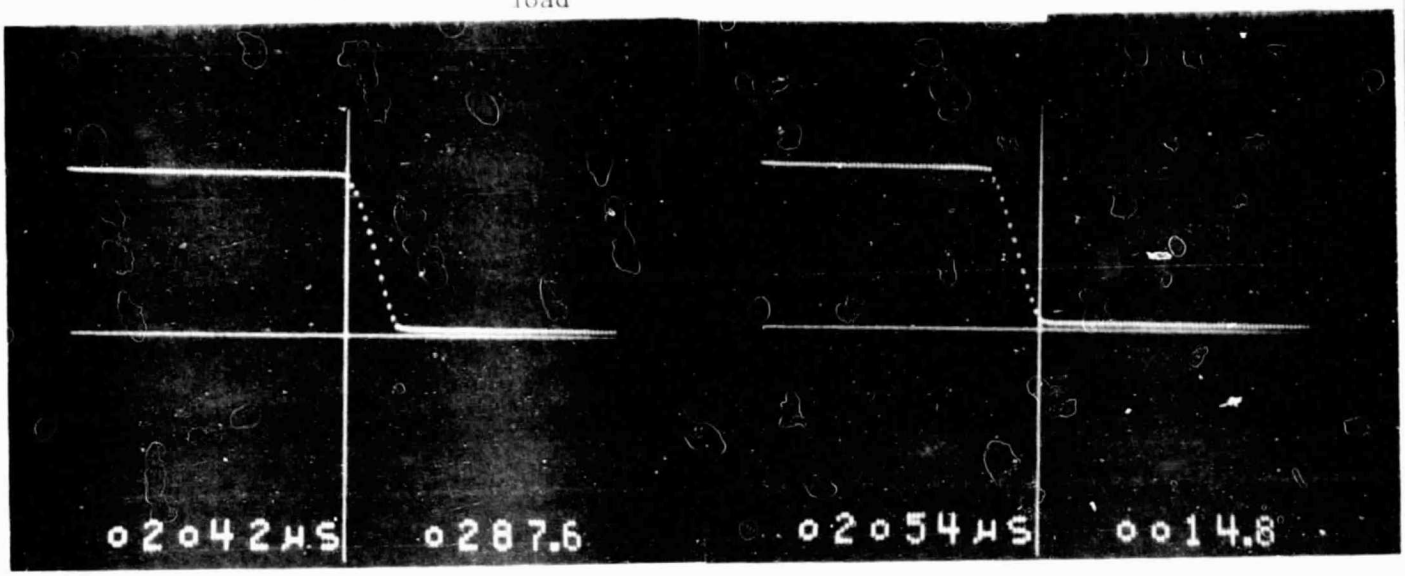
FIG. 9-14 AVC-43 SSPC VACUUM PERFORMANCE TEST
TEMPERATURE Vs TIME
10-5 torr
TEMPERATURE, DEGREES C
120
100
80
60
40
20
0
10
20
30
40
50
60
70
80
90
TIME, MINUTES
D60T
12°
Heat Sink Top
17°
Heat Sink Bottom
16°
SSPC BASE
61°
COLD PLATE

Figure 9-15

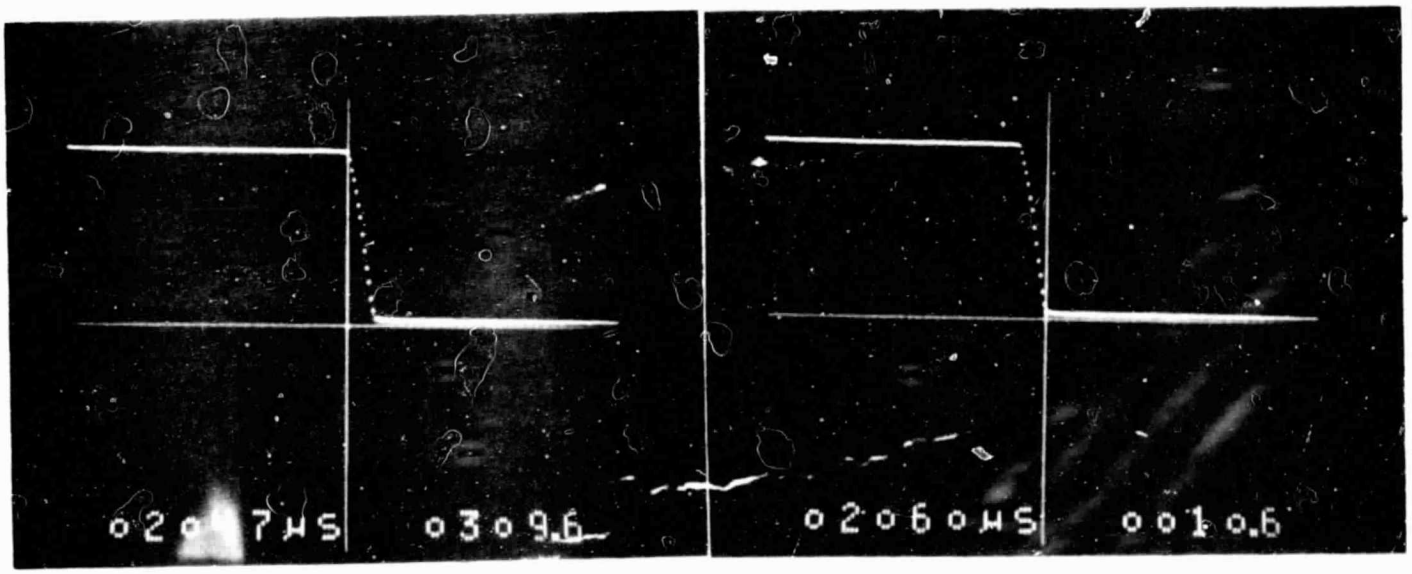
Vacuum Chamber Test

SSPC Switch Voltage Turn-On Waveforms

VDC = 300V, I_{load} = 50A



Turn-On at Laboratory Ambient: T (ON) = 2.04 msec., T (fall) = 12 µsec.



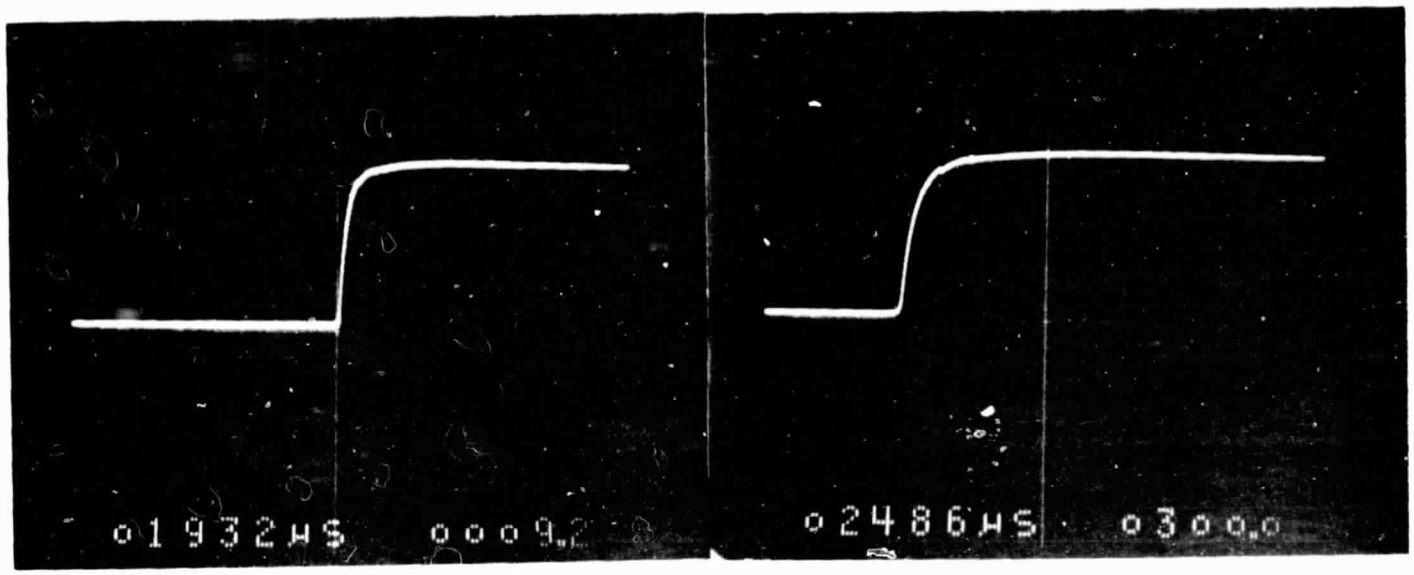
Turn-On at 10^{-5} torr: T (ON) = 2.05 msec., T (fall) = 13 µsec.

Figure 9-16

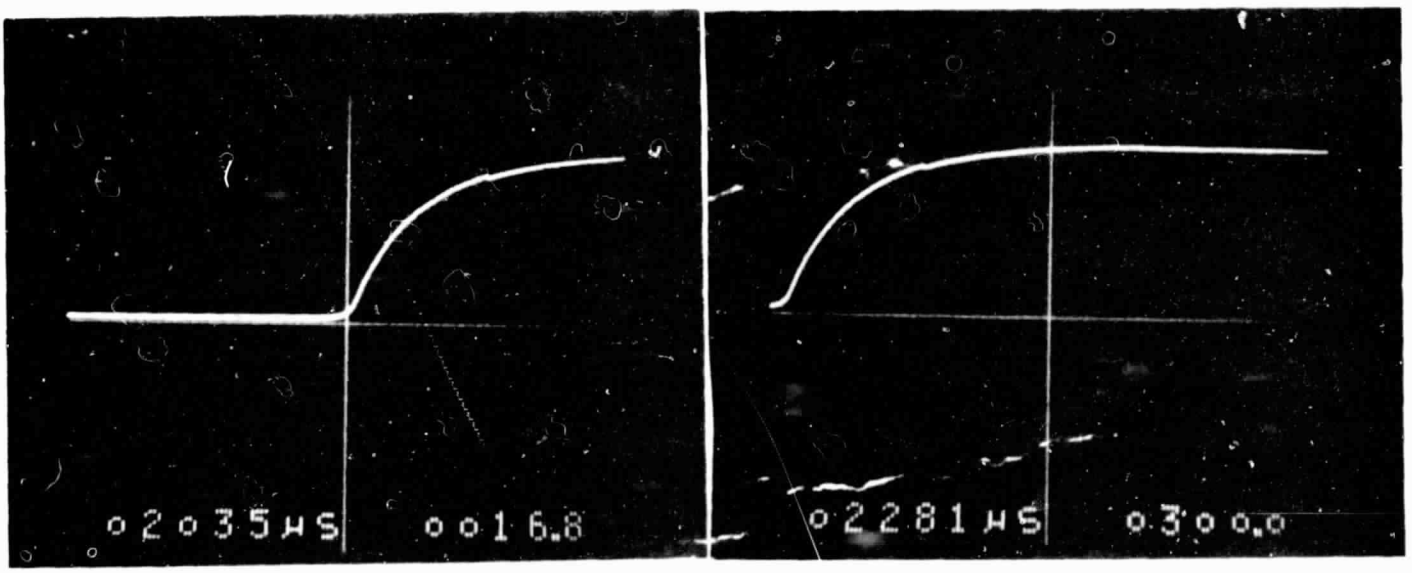
Vacuum Chamber Test (Continued)

SSPC Switch Voltage Turn-Off Waveforms

VDC = 300V, I_{load} = 50A



Turn-Off at Laboratory Ambient: T (OFF) = 1.93 msec., T (rise) = 554 µsec.

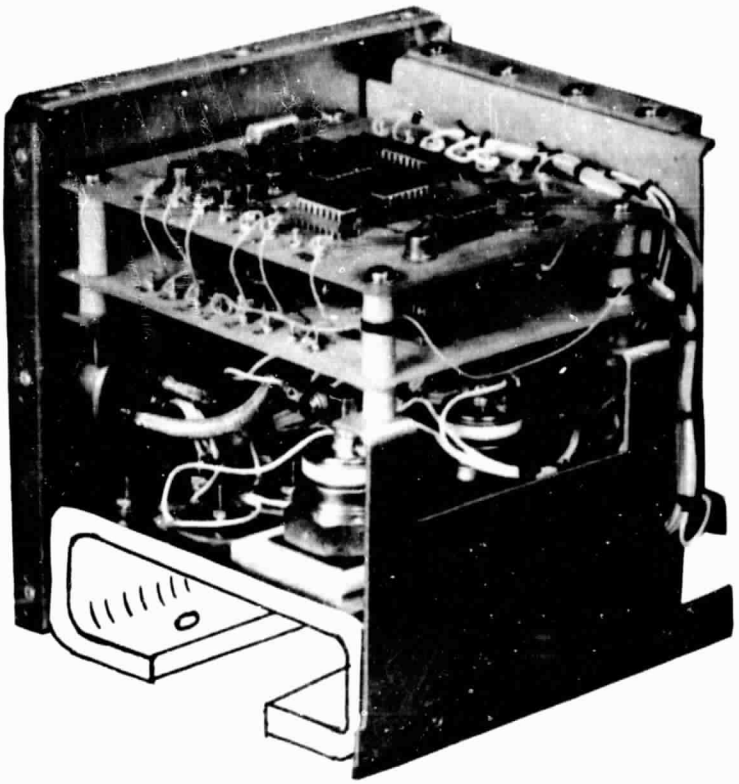


Turn-Off at 10^{-5} torr: T (OFF) = 2.35 msec., T (rise) = 246 µsec.

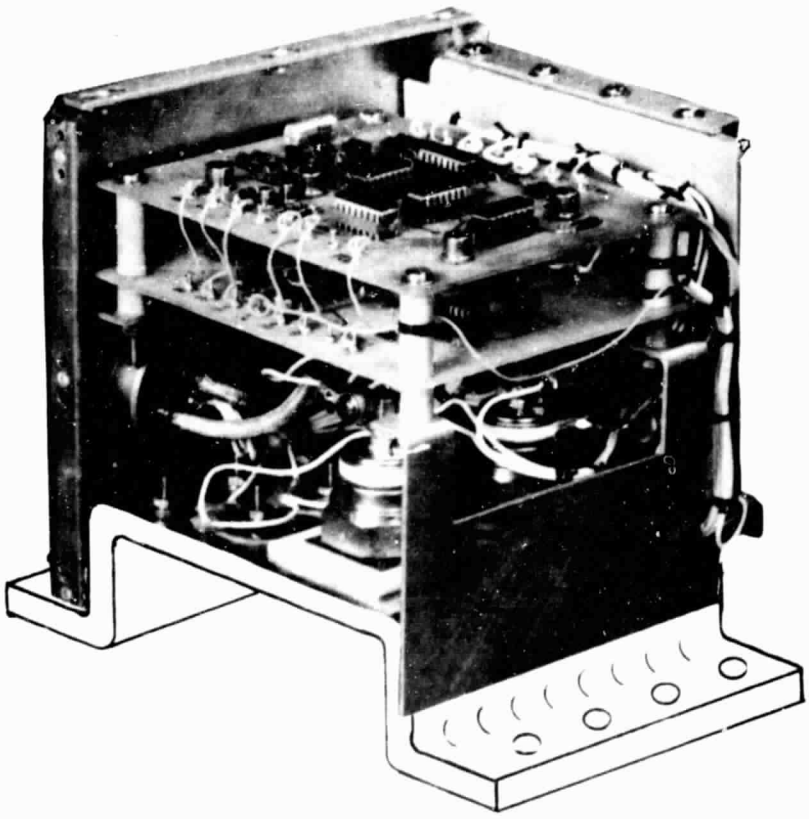
9.4.3 Design Recommendation

The SSPC packaging design used conventional packaging/mounting techniques in meeting both bench and vacuum chamber performance requirements. While the mounting surface temperature of 10°C (50°F) required to maintain the power transistor junction temperature at a safe value is not too unreasonable, it might be justified to consider a unitized or integrated base heat sink and a higher quality finish on the SSPC base mounting surface interface. This would eliminate heat sink base interface and reduce the thermal drop between the SSPC base and the mounting surface which accounted for 76°C of the 95°C thermal rise from mounting surface to the power transistors. Figure 9-17 depicts a modified SSPC base heat sink design utilizing finishes of 16 microinch CLA (polish) with .00050 in./in. flatness on both SSPC base and the mounting surface. With a dry interface (i.e., no thermal compound or material) and a torque of 30 in.-lbs. (8.5 N-M), the calculated thermal characteristics are as follows:

θ (D60T - Heat Sink)	.11°C/W
θ (Heat Sink - Base)	.27°C/W
θ (Base - Mounting Plate)	.18°C/W
θ (D60T - Mounting Plate)	.56°C/W
Max. Mounting Plate Oper. Temp. for T (D60T) of 105°C	43°C



a. Inward Flange Design



b. Outward Flange Design

Figure 9-17

50A/400 VDC SSPC With Integral Base and Heat Sink

APPENDICES

TABLE OF CONTENTS

APPENDIX A

DESCRIPTION

TYPE AVC-45
SOLID STATE POWER CONTROLLER

DC LOAD SWITCHING SPST-NO
25 AMPERES, 500-1100VDC

APPROVAL	DATE
Engineer	6-17-80
Design Sect. Mgr.	6-18-80
Marketing Syst. Mgr.	
Qual. & Rel. Engrg.	
Supv. Standards	

REVISIONS

WESTINGHOUSE ELECTRIC CORP.
AEROSPACE ELECTRICAL DIV.
LIMA, OHIO, U. S. A..

REV.	CODE IDENT NO
	83843
DESIGN SPEC. NO.	D-774154
SHEET 1 OF 5	

ELECTRICAL CHARACTERISTICS (-40 to 100°C ambient temperature unless otherwise specified)

General

Circuit arrangement	SPST NO
Insulation resistance	100 megohms minimum
Dielectric withstanding voltage	Applicable, 2000VAC, 1 min.
Isolation	Applicable, 2000VAC, 1 min.
Life (operating cycles)	10^6 minimum
Radio interference	Applicable
Leakage current	10.0 milliamperes maximum
Power dissipation (rated load)	
"ON"	40W
"OFF"	12W
"TRIPPED"	12W
Efficiency at 500V/25A DC Load	
Minimum	99.6%

Power Circuit

Operating Supply Voltage	500-1100VDC
Switch Voltage Drop	1.5VDC maximum (25°C)
Rupture Capacity	50 amperes minimum (500-1100VDC)
Fault Protection	500-1100VDC operation: Per Fig. 1 500VDC operation: Buss Fuse # NOS. 35
Trip Free	Applicable

Response Times

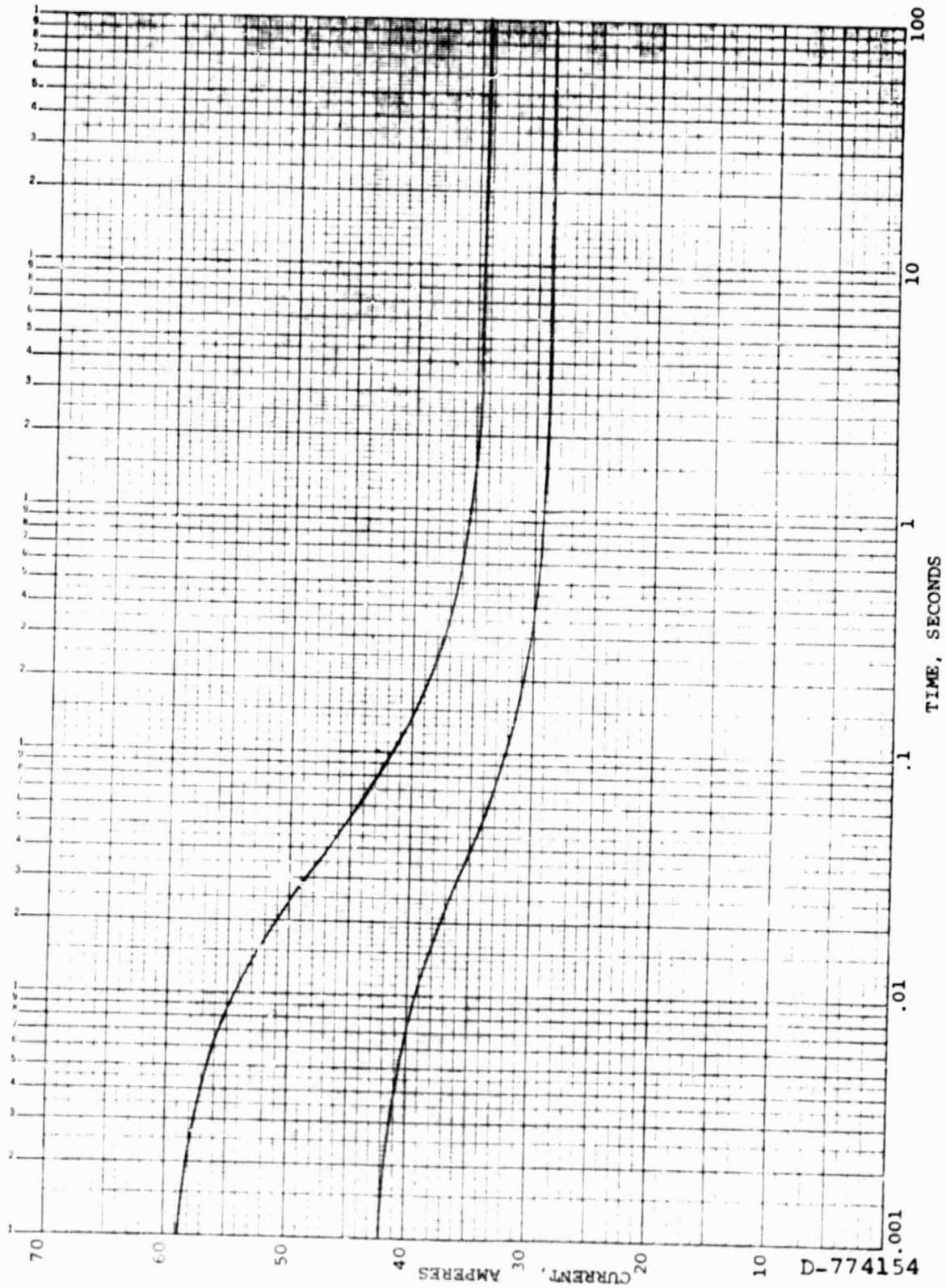
Turn-On and Turn-Off	10.0 ±5.0 milliseconds
Commutation	128 ±10.0 milliseconds
Time between Operations	153 milliseconds minimum
Power-Up Turn-On Time	20 milliseconds maximum

Control Circuit

Supply Voltage	28 ±7VDC
Supply Current	.13ADC maximum
Supply Voltage UV Protection	19.0 ±1.0VDC with 8.0 ±2.0 milliseconds time delay
Control Command "ON" Voltage	4 volts DC maximum
Control Command "OFF" Voltage	2 volts DC maximum
Control Command Voltage	13 volts DC maximum (open circuit
Control Command Current	15ma DC maximum (short circuit)
OC Lockout Reset Means	Removal of control command voltage
Removal Time to Reset	10.0 ±5.0 milliseconds

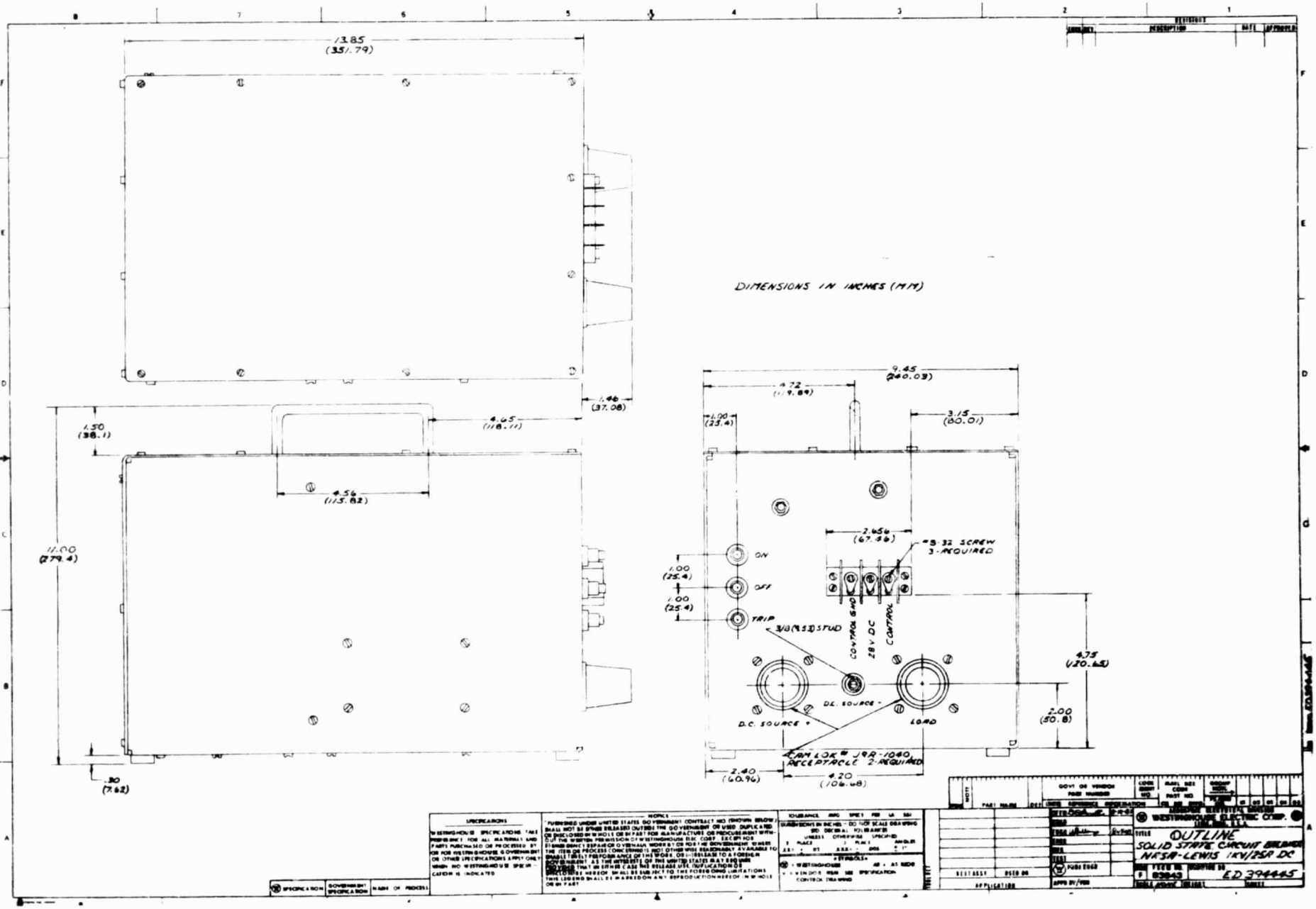
Indication (Front Panel)

"ON" State (Load Energized).....	GREEN LED "ON"
"OFF" State (Load De-energized)..	CLEAR LED "ON"
TRIPPED State (Subsequent to Overcurrent Trip)..	CLEAR AND RED LED's "ON"



Sheet 4 of 5

Figure 1. Overcurrent protection 1KV/25A DC SSPC Breadboards 500V - 1100V operation



A-5 D-774154 Sheet 5 of 5

APPENDIX B

DESCRIPTION

TYPE AVC-41
LATCH-TYPE CIRCUIT BREAKER
WITH SOLID STATE COMMUTATION

DC LOAD SWITCHING, SPST-NO
80 AMPERES, 200-400VDC

APPROVAL	DATE
Engineer W Billings	2-7-80
Design Sect. Mgr. R Swanson	2/11/80
Marketing Syst. Mgr.	
Qual. & Rel. Engrg.	
Supv. Standards	

REVISIONS	
ADD S.I. UNITS 7-23-81 JJ Marshall	

WESTINGHOUSE ELECTRIC CORP.
AEROSPACE ELECTRICAL DIV.
LIMA, OHIO, U. S. A.

REV.	CODE IDENT NO. 83843
DESIGN SPEC. NO. D-774147	
SHEET 1 OF 3	

PERFORMANCE SPECIFICATIONS

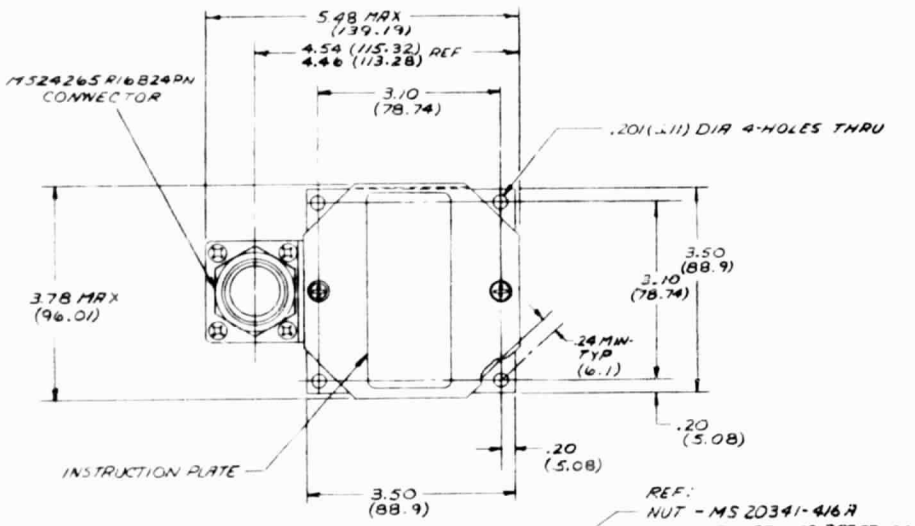
Main Contact:	SPST-NO
Rated Voltage	200-400VDC
Maximum Operating Voltage	450VDC
Continuous Current	80 Amperes
Interruption Maximum	100 Amperes
Commutation Method	Transistor Transfer
Volt Drop at 80A	.20 Max.
Latch Mechanism:	P. M. Type
Auxiliary Contacts:	4 Form C
Voltage DC	30 Volts
Current Resistive	7.5 Amperes
Current Inductive	7.5 Amperes
Voltage AC	125 Volts
Current AC	7.5 Amperes
Temperature Range:	-55°C to 71°C Ambient
Operating Voltage Maximum/Minimum:	30/15 Volts
Operating Time (Seconds at 25°C - Close:	.025 Seconds at 15 Volts
Trip:	.025 Seconds at 15 Volts
Number of Operations:	TBD
Close Coil Res:	3.4 Ohms
Trip Coil Res:	3.4 Ohms
Weight:	3.5 lbs. est.
Size: (L x W x H)	5.48 x 3.50 x 5.87
Stud Size:	1/4 - 28 UNF-2A
Connector:	MS 24265 R16B24PNX

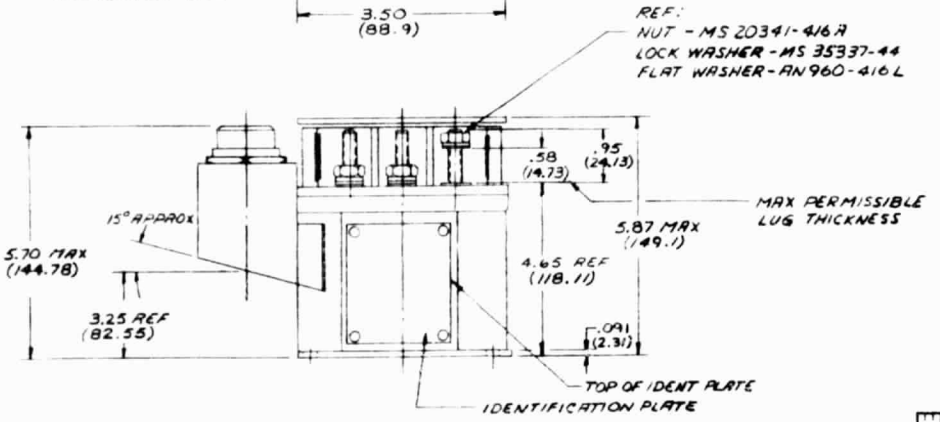
PDS NO. ED394441 SH

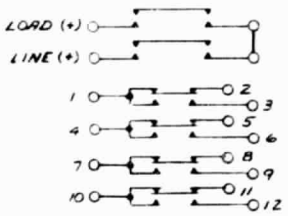
REVISIONS

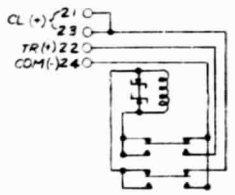
ZONE	REV	DESCRIPTION	DATE	APPROVED

1. DIMENSIONS IN INCHES (M M)









SCHEMATIC DIAGRAM

SPECIFICATION	GOVERNMENT SPECIFICATION	NAME OF PROCESS

SPECIFICATIONS

WESTINGHOUSE SPECIFICATIONS TAKE PREFERENCE FOR ALL MATERIALS AND PARTS PURCHASED OR PROCESSED BY OR FOR WESTINGHOUSE GOVERNMENT OR OTHER SPECIFICATIONS APPLY ONLY WHEN NO WESTINGHOUSE SPECIFICATION IS INDICATED

NOTICE

FURNISHED UNDER UNITED STATES GOVERNMENT CONTRACT NO. (SHOWN BELOW) SHALL NOT BE EITHER RELEASED OUTSIDE THE GOVERNMENT, OR USED, DUPLICATED OR DISCLOSED IN WHOLE OR IN PART FOR MANUFACTURE OR PROCUREMENT WITHOUT THE WRITTEN PERMISSION OF WESTINGHOUSE ELEC. CORP. EXCEPT FOR EMERGENCY REPAIR OR OVERHAUL WORK BY OR FOR THE GOVERNMENT, WHERE THE ITEM OR PROCESS CONCERNED IS NOT OTHERWISE REASONABLY AVAILABLE TO ENABLE TIMELY PERFORMANCE OF THE WORK, OR (ii) RELEASE TO A FOREIGN GOVERNMENT AS THE INTERESTS OF THE UNITED STATES MAY REQUIRE PROVIDED THAT IN EITHER CASE THIS RELEASE USE, DUPLICATION OR DISCLOSURE HEREOF SHALL BE SUBJECT TO THE FOREGOING LIMITATIONS THIS LEGEND SHALL BE MARKED ON ANY REPRODUCTION HEREOF IN WHOLE OR IN PART

TOLERANCE MFG SPECS PER LA 551

DIMENSIONS IN INCHES - DO NOT SCALE DRAWING
3RD DECIMAL TOLERANCES
UNLESS OTHERWISE SPECIFIED

2 PLACE	3 PLACE	ANGLES
XX= ± .02	XXX= ± .005	± 1°

+SYMBOLS+
W = WESTINGHOUSE AE = AS REQD
V = VENDOR ITEM SEE SPECIFICATION CONTROL DRAWING

NOTE	PART NAME	DES	GOVT OR VENDOR PART NUMBER (SIZE) REFERENCE INFORMATION	CODE IDENT NO.	MATL SIZE CODE PART NO OR SPEC TYPE	GROUP NOTE	01	02	03	04	05
			DRTD								
			CHKD								
			ENGG								
			MFG								
			QUA								
			TEST								
			PROJ ENGR								
			APPD BY/DATE								

BEST ASSY | USED ON
APPLICATION

AEROSPACE ELECTRICAL DIVISION
WESTINGHOUSE ELECTRIC CORP.
LIMA, OHIO, U.S.A.

TITLE
OUTLINE
MFR TYPE AVC-41

SIZE D | FSCM NO. 69843 | DRAWING NO ED 394441

SCALE AVOMK | WEIGHT | SHEET

APPENDIX C

DESCRIPTION

**TYPE AVC-43
SOLID STATE POWER CONTROLLER**

**DC LOAD SWITCHING SPST-NO
50 AMPERES, 200-400VDC**

APPROVAL	DATE	REVISIONS
Engineer W Billings	3·13·80	A
Design Sect. Mgr. R.E. Stranger		B
Marketing Syst. Mgr.		
Qual. & Rel. Engrg.		
Supv. Standards		

WESTINGHOUSE ELECTRIC CORP.
AEROSPACE ELECTRICAL DIV.
LIMA, OHIO, U. S. A.

REV.	CODE IDENT NO. 83843
DESIGN SPEC. NO.	D-774149
SHEET 1 OF 5	

ELECTRICAL CHARACTERISTICS (-40 to 100°C ambient temperature unless otherwise specified)

General

Circuit arrangement	SPST NO
Insulation resistance	100 megohms minimum
Dielectric withstanding voltage	Applicable, 1500VAC, 1 min.
Isolation	Applicable, 1500VAC, 1 min.
Life (operating cycles)	10^6 minimum
Radio interference	Applicable
Leakage current	5.0 milliamperes maximum
Power dissipation	
"ON"	100 watts
"OFF"	5.0 watts
"TRIPPED"	5.0 watts
Efficiency	
Minimum	99.0%
Objective	99.5%

Power Circuit

Supply voltage	200-400VDC operating 500VDC maximum peak transient
Current	
Rated (no load to 100% rated)	50 amperes dc
Voltage drop (no load to rated)	1.90 volts dc maximum
Rupture capacity	500 amperes minimum
Overshoot circuit	
Amplitude	3000% of rated current maximum
Time	10 microseconds maximum
Fail safe I^2t	62,500
Response	
Turn-on time	.01-10 milliseconds
Rise time	.01-.50 milliseconds
Turn-off time	.01-10 milliseconds
Fall time	.01-1.0 milliseconds
Trip free	Applicable
Trip time	
Nonrepetitive reset	See Figure 1
Repetitive resetting	30 seconds minimum between resets

Control Circuit

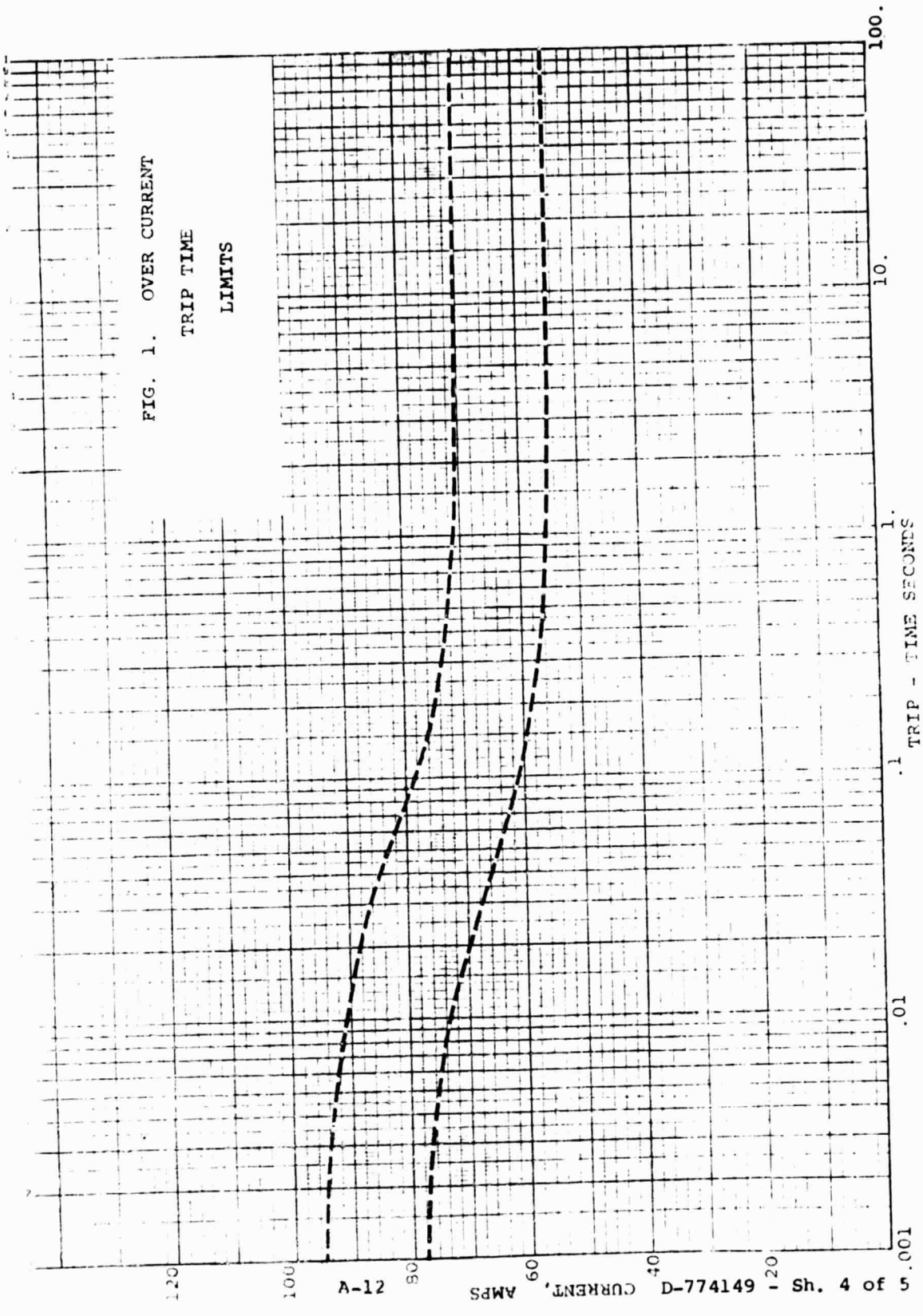
Supply Voltage.....	28 ±7 volts dc
Supply Current.....	150 milliamperes dc maximum
Turn-On Voltage.....	4.0 volts dc maximum
Turn-Off Voltage.....	2.0 volts dc minimum
Input Current.....	10.0 milliamperes maximum at 6VDC
Input Transients.....	Applicable
Removal Time to Reset.....	5.0 milliseconds minimum
.....	20.0 milliseconds maximum

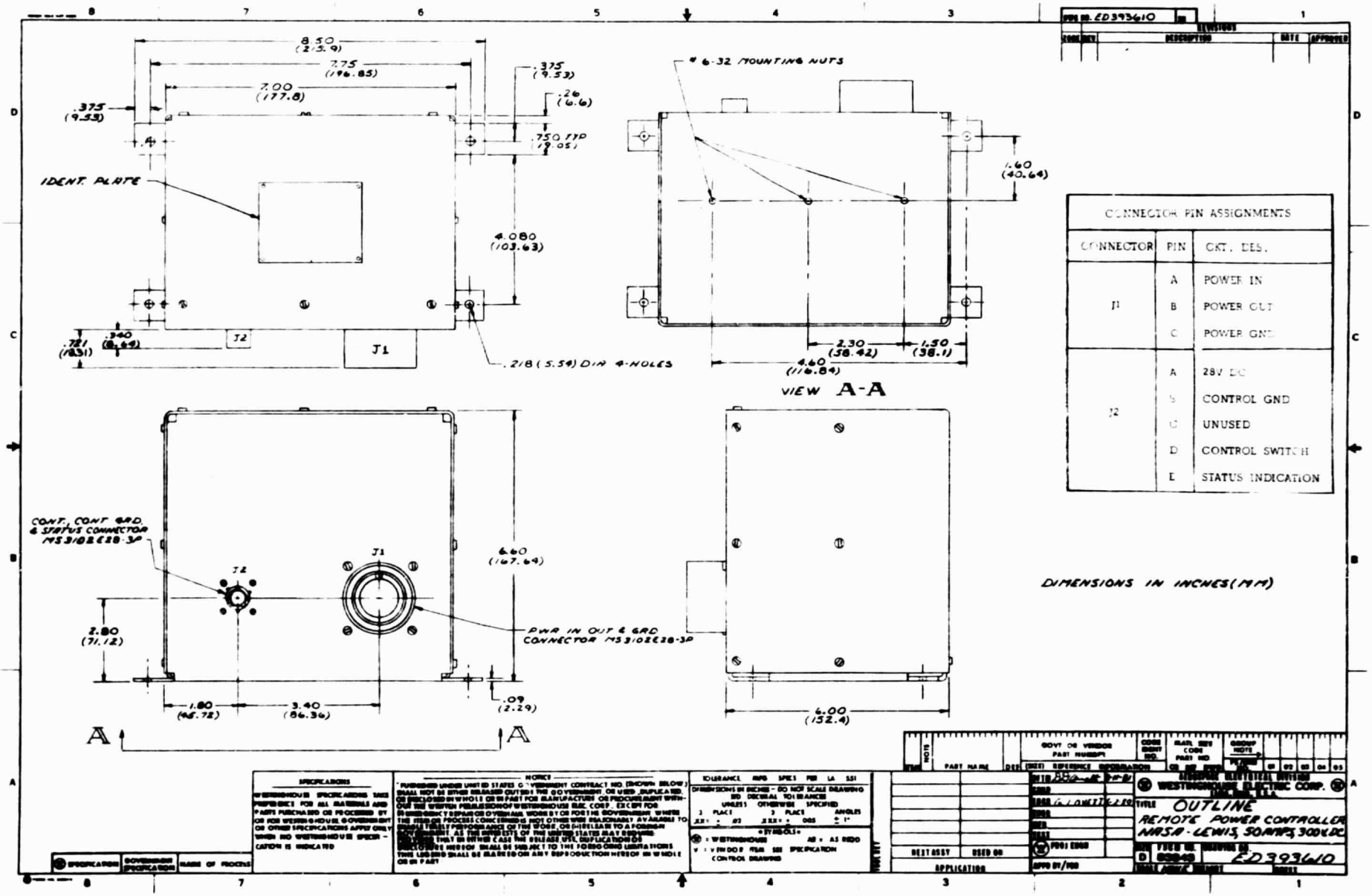
Undervoltage Protection

Operating Level.....	18.0 ±3.0 volts dc
Time Delay.....	5-15 milliseconds

Status Indication Signal

Tripped.....	0.5 volts dc max. when sinking .040 milliamperes max.
Not Tripped.....	10 microamperes max. leakage at 30 volts dc





CONNECTOR PIN ASSIGNMENTS		
CONNECTOR	PIN	CKT. DES.
J1	A	POWER IN
	B	POWER OUT
	C	POWER GND
J2	A	28V DC
	B	CONTROL GND
	C	UNUSED
	D	CONTROL SWITCH
	E	STATUS INDICATION

WESTINGHOUSE ELECTRIC CORP.
TITLE OUTLINE
REMOTE POWER CONTROLLER
NASA - LEWIS, 50 AMPS, 300V DC
ED393610

A-13 D-774149 Sheet 5 of 5